1. Introduction to HiRelPCI

This is an introduction to a IEEE P1996 to define a:

Standard for an Extendible High Reliability Enhanced PCI Bus.

This bus came from a need to provide a High Reliability, High Availability system for transportation control and telecommunications systems. Transportation and traffic control have a need for very low system failure rate in difficult environments. These system must operate on the street corners from northern Alaska to the southern deserts of Arizona with the extremes of temperature and humidity prevalent to such locations. The telecommunications requirements are not quite as severe in the environmental area, but are similar in the need for R.A.M. (Reliability, Availability and Maintainability) plus the additional need of a Time Division Multiplexed bus for circuit switched data using elements of the international Synchronous Digital Hierarchy (SDH) at rates defined in ANSI T1.105-1991. Both areas of usage need redundant capabilities to allow continued operation with a single fault. Additional areas of interest for this project are Process Control, Communications, and embedded systems. Maintenance function utilize the MTM bus structure as defined in IEEE Std 1149.5-1995 with compatible extensions.

These application areas need a method of extending beyond the local bus to other similar buses in a uniform, redundant manner. The solution to this need was to include a provision in the bus to handle the message packets of the IEEE Std 1394-1995, IEEE P2100 Serial Express and IEEE Std 1596-1992 SCI. This addition provides for 64K addressable nodes and a uniform 64 bit address space. In more demanding multiprocessor systems, the cache coherency methods of SCI can be employed as needed.

This bus is designed to satisfy these needs.

FEATURES OF THIS HiRelPCI BUS

The following set of features of the P1996 HiRelPCI Bus drive its utility:

Reliability - Through passive backplane, Redundant Buses, Redundant power
Availability - Through design for NO Single Point of Failure
Maintainability - Through MTM bus, Hot Swap, Standby modules
Scalability - Through PacketBus to P2100 and SCI, Circuit Switch I/O through STS-12
Performance - PacketBus performance to 533 MByte/second with up to 95.5% efficiency
Redundancy - no single point of failure on a normally configured system.
-40C to +85C Industrial/Automotive temperature range operation
Power Distribution at nominal 48V for highest efficiency
Configuration Management through CSR Architecture, Serial Express and MTM busses
Redundant connectivity through backplane Firewire and 10Base2 Ethernet

1.1 ELEMENTS OF HiRelPCI BUS

This bus standard is a combination of elements taken from other elements and modified to provide the structure to meet the needs described above. The elements that make up this high reliability, high availability bus include:

1. A Parallel system bus using PCI style signaling for normal bus access
2. A PacketBus added on top of the Parallel system bus for packet switched connections
3. A Time Domain Multiplexed bus for circuit switched connections
4. A maintenance bus for control of system resources for hot swap operations
5. An Addressing structure that uses the standard 64 bit address space
6. Several supporting interconnection systems
7. A set of electrical specification for low voltage signaling, 3.3V PECL signaling and power

8. A set of mechanical specifications to provide a well defined enclosure system

The combination of these elements build a system that provides:

1. Extensibility to 64K nodes of 256 Terabytes each
2. IEEE 1212-1991 CSR Architecture for easy expansion via SCI, Serial Express,1394-1995 etc.
3. Redundant functions to provide no single point of failure for continuous operation
4. Hot Plug of any board to replace faulty modules or update features.
5. Circuit Switched base for Audio, Telephony, Video, ATM for consistent external/internal model
6. Packet Switched connection model for shared memory operations via SCI/CSR internal/external

1.2 Bus Signal Definitions

Nominal bus signaling on the P1996 is based on the PCI Local Bus Specification 2.1 using 3.3V signal levels. This provides leverage on all the silicon built to support the PCI market. This protocol is flexible and provide performance from 0 - 533 megabytes per second with the addition of Packet Write burst transactions.

This bus has been extended to include a packet mode, called PacketBus, to support the packets sent over the SCI/Serial Express busses to extend transparent communications to other elements of a distributed, redundant system. Packet operations are transparent to the normal PCI transactions compliant to Rev 2.1. HiRelPCI bus can operate in PacketBus, normal PCI mode or a mix of both modes. PacketBus mode of operation can be used to expand the normal PCI functions and has been proposed to the PCI technical committee for inclusion in the future PCI Local Bus specifications.

Transparent operation is accomplished with the addition of a command mode on the PCI that is a write only mode. In this mode the packet is a write on the bus with the high order 16 bits being used as an address for one or more nodes to capture or indicate the failure to capture. Write Only operations are supported in both 32 and 64 bit wide operations that will deliver the bit serial equivalent of 4.266 gigabits per second.

Today’s limitation on the driver technology and the physics of the backplane restrict the number of backplane segment positions to 7, or 8 when stretched. Extensibility is required to extend the operation to additional nodes in systems attached through SCI/Serial Express links.

Each component in the system is attached to the Maintenance Bus which is a bus defined by the IEEE Std 1149.5-1995 documents. Maintenance Bus signal lines are:

Table 1—Maintenance Bus Signals

Signal Name	Signal Function	Signal Direction
MCLK	MTM Clock	To all from CSM
MMD	Master Data	From Master
MSD	Slave Data	To Master
MPR	Master Pause Request	To Master
MCTL	Master Control	From Master

1.3 Parallel Bus Operations

In addition to the normal PCI style operation, additions and deletions have been made to improve the operation of the bus. Specific additions have been the prioritized bus request facilities, PacketBus, the MTM maintenance bus, 48VDC power, constant clock, backplane Ethernet and Firewire. Specific deletions are INTA#, INTB#, INTC# and INTD#, 5VDC and 3.3VDC power.

1.3.1 CSM Functions

Centralized resources needed for bus operations are supplied by the Central Services Module. There shall be one CSM for each bus segment. In most cases, a CSM will span two HiRelPCI buses in the 12su configurations and only one bus in the 6su configuration. This module provide all the clocking and arbitration for the parallel bus and the TDM bus when present.

The Central Services Module provides the following services for the bus:

Clock drivers for each slot on the bus segment
Bus Arbitration for each slot on the bus segment
Repeater Hub for the Ethernet signals
Repeater Hub for the 1394 Firewire serial bus
Possible Bridge to IEEE P2100
PCI to PCI Bridge if needed
Possible TDM interface between outside world and backplane bus
TDM to TDM Bridge and framing store if needed
Clocks for the TDM slots when used
System monitor functions
Maintenance Bus Master

1.3.2 Priority Bus Request Mechanism

This provides a prioritized request in addition to the normal round robin Fairness priority system of the PCI bus. This priority scheme uses four pins REQP0# to REQP3# to define the priority level of each bus request as level 0 to 15. Bus request are issued at the rising edge of FRAME# by activating their REQ# and priority level on REQP[3::0]#. The priority level on the bus for this cycle is seen by all participants. Lower level requesters will retire and remove the REQ# if a higher level request is pending. The CSM arbiter determines the winner or winners and issues the bus grants to the boards with the highest level of priority on a round robin basis and then to the next lower level of priority on a round robin basis until there are no pending bus requests.

Prioritized bus requests may have 1 to 8 requests pending at any given level of request, the requests are granted in round robin priority until all are issued while building a queue at the same level to insure fairness within the bus request queueing level. This also guarantees priority among the bus request queueing levels.

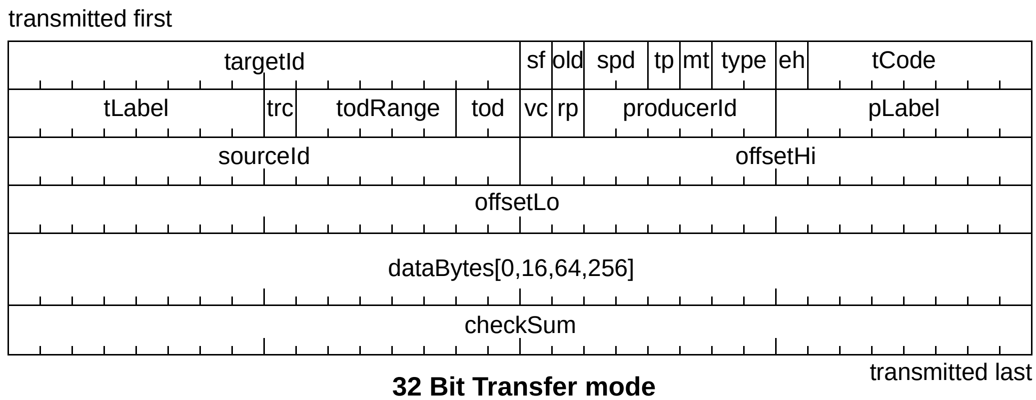
Boards using the PCI style single REQ# line will request at bus request level 0. Any higher level of request will block the lower level request. This mechanism is transparent to the single level request mechanism and will be seen as a possibly longer delay until a GNT# is received.

1.4 PacketBus Operations

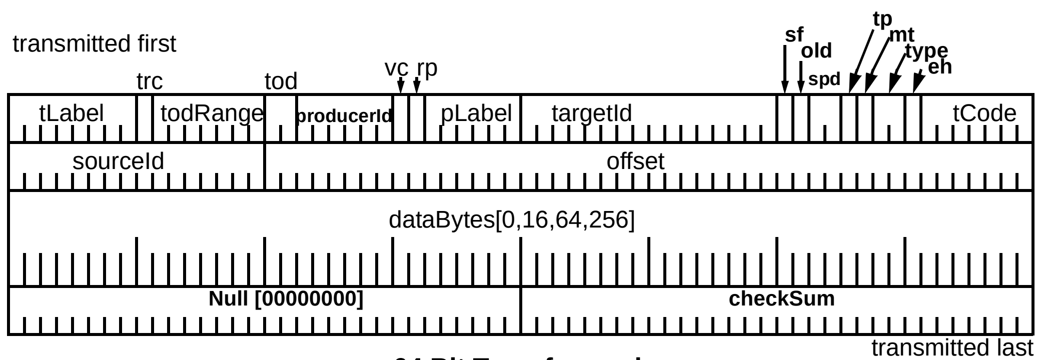
PacketBus operations are added to the basic parallel bus structure to improve the performance of the system with a split response mode of operation. This mode is also known as a write only mode of bus operation in that each request and response is a write transaction. The basic function is to free the bus resource during the time needed to fetch or process the data at the target end of the transaction. Packet mode operation does impose additional requirements on the participants as buffers are needed to handle the packets to and from the bus.

PacketBus operation is optional for the HiRelPCI bus. This mode can be used to produce the highest bandwidth operations on the bus with greater than 4 gigabit throughput a reality.

PacketBus operations require the use of a new command mode in the PCI specification and the redefinition



32 Bit Transfer mode



64 Bit Transfer mode

of several of the PCI signal lines during this mode of operation. In all cases these changes are transparent to the existing PCI devices.

The preferred command mode is the “0101” mode which would be an unused WRITE transaction. Current devices are required by PCI Local Bus Specification Revision 2.1 to ignore this command code and hence no interference with the existing operations. These packets are of the general form shown the Figure above.

A command field identifies the different forms of send packets, as described in the chapter on the Packetbus.

1.4.1 CSR Space Mapping

This standard adheres to the IEEE Std 1212-1992 Control and Status Register Architecture standard using the 64bit fixed address model.

1.5 TDM Bus Operations

Dual TDM busses are included as an option for Telecommunications usage. These busses share a common clock and frame signal. Each TDM block consists of 6 ground pins, 1 clock pin, 1 frame pin and 2 sets of 8 data lines. The clock pin is routed individually to each slot to provide tight timing specification.

This bus will follow the structure of ANSI T1.105-1991 SONET (as revised) using the blocking factors used in the international standard. This standard provides a reference for multiple embedded carriers and provides an internationally accepted framework for circuit presentation and ATM integration if needed. Basic timing is provided by the CSM board position and consists of clocks with less than 1 ns of skew and a framing pulse to define the local chassis time slot count. Adjustment may be made to synchronize with one external source of framing information. The first 24 time slots are used for synchronization purposed and to move the relative frame time on different parts of the system to be in coordination with the backplane requirements though frame buffers and other necessary techniques.

The overhead portions of the ANSI SONET standard are not yet specified

Simulations indicate possible clock speeds to 77.76 MHz using 3.3V PECL logic to provide an upper limit of STS12 on each of the sets of data lines.

12su systems would have dual TDM blocks for reliable redundant operation. Each of these busses has 2 byte wide paths that may be used as input and output streams and are each readable and writable on each time period. Each cycle is 12.86 ns in duration which requires terminated 3.3V PECL bus to reduce reflections and lower the propagation delay to incident wave travel.

1.6 Maintenance Bus Operations

The Maintenance Bus Master issues sets of commands that are fully described in the IEEE Std 1149.5-1995. These commands are summarized in the following table.

In addition to the normal commands provided by the 1149.5 command set, the command extension

Table 2—Maintenance Bus Commands

Command Class	Command Code (Binary)	Command Code (HEX)	Command	Status
Core	0000000	00	Read Status	Required
	0000001	01	Abort	Required
	0000010	02	Reset Slave Status	Required
	0000011	03	Contend for Bus	Required
	00001XX	04-07	Multicast Group Select	Required
	0001000	08	Enable Idle Interrupts	Required
	0001001	09	Enable Pause Interrupts	Required
	0001010	0A	Disable Idle Interrupts	Required
	0001011	0B	Disable Pause Interrupts	Required
	0001100	0C	Enable Module Control	Required
	0001101	0D	Data Echo Test	Required
	0001110	0E	Verify BMR	Required
	0001111	0F	Initialize Application	Required
	0010000	10	Disable Module Control	Required
	0010001	11	Start	Required
	0010010-0011111	12-1F	Reserved	Reserved
	1111111	7F	Illegal Command	Required
Data Transfer	0100000	20	Read Data	Recommended
	0100001	21	Write Data	Recommended
	0100010	22	Read/Write Data	Recommended
	0100011-010111	23-27	Reserved	Reserved
Module Initialization and Self-Test (MIST)	0101000	28	Reset Module with SBIT	Recommended
	0101001	29	Reset Module without SBIT	Recommended

Table 2—Maintenance Bus Commands

Command Class	Command Code (Binary)	Command Code (HEX)	Command	Status
	0101010	2A	Module IBIT	Recommended
	0101011-0101111	2B-2F	Reserved	Reserved
Module I/O Control and Test (MICT)	0110000	30	Disable Module I/O	Recommended
	0110001	31	Enable Module I/O	Recommended
	0110010	32	Force Module Outputs	Recommended
	0110011	33	Sample Module-No Change	Recommended
	0110100	34	Sample Module-Don't Care	Recommended
	0110101	35	Sample Module with Force	Recommended
	0110110	36	Release Module I/O	Recommended
	0110111-1001111	37-4F	Reserved	Reserved
Standard Extension	1010000-1011111	50-5F	Reserved for use of standards making bodies	Reserved
HiRelPCI Extensions	1010000	50	Disconnect module from HiRelPCI Bus	Required
	1010001	51	Connect Module to HiRelPCI Bus	Required
	1010010	52	Disable main power converters	Required
	1010011	53	Enable main power converters	Required
	1010100	54	Read Serial Number, NodeId	Required
	1010101	55	Read PCI configuration space	Required
	1010110	56	Write PCI configuration space	Required
	1010111	57	Read Power Status Block	Required
	1011000	58	Set Poke Address and mode (64 bits)	Required
	1011001	59	Read Poke Data (64 Bit mode)	Required
	1011010	5A	Write Poke Data (64 bit mode)	Required
	1011011	5B	TBD	Required
	1011100	5C	Read 1149.1 JTAG data	Required
	1011101	5D	Write 1149.1 JTAG Data/Program Data	Required
	1011110	5E	Read Message (Header + Data + CRC)	Required
	1011111	5F	Write Message (Header + Data + CRC)	Required
User-Defined	1100000-1111110	60-6E	User-Defined Commands	Reserved

for HiRelPCI are added as commands 50 to 5F.

The Maintenance Bus (abbreviated MTM in this document) is attached to all elements in a common chassis. This extends to all boards, power supplies and fans that support a physical backplane which may contain up to 2 segments. The IEEE Std 1149.5 MTM bus that uses 5 signal lines and has been defined for use in Avionics an other similar systems use by the same standards group the provided the IEEE 1149.1 JTAG testing functions.

Required functions:

Read Board Unique Identifier
Read Board Configuration ROM (or other device
Read Board Slot Identifier (SAD lines)
Connect and disconnect Board from Bus
Control Power on board
Perform Built In Self Test (BIST) functions
Perform the JTAG Testing of the board
Read/Write IEEE 1212-1991 Address space
Control diagnostic systems testing such as induced failures
Other functions as defined by the board designer

1.7 CSR Specifications and Configuration Operations

1.7.1 Node Addressing

Extending beyond a single PCI style bus is required for applications that need more or vastly more processors, memory and I/O boards. Redundant operations also require more than one processor, memory and I/O board. Connectivity beyond a single system is greatly enhanced by addressing a card slot on a bus segment as a node. Each slot has a node address consisting of 16 bits, split into 3 bits of slot-id and 13 bits of address assigned by a switch on the backplane or by a bridge to the SCI/P2100 node address. While this does allow 8192 bus segments of 8 slots/nodes each, the use of all slots within a backplane environment will define up to 16 slots/nodes for each chassis and limit the number of chassis to 4096. P2100 bus addressing which is defined around 1024 buses of 64 nodes each and makes specific allowances to support more busses of less nodes. All addressing for normal operation is directed to 16 bit nodeId which are routed to the proper bus and node.

These 16 pins are distributed along the connector and bypassed to ground, or connected to ground to provide a high quality signal return path.

IEEE 1212-1991 addressing is used with these 16 bits defining a slot as one of the 65536 in the address space. Each node has a sub address range of 48 bits for total address space of 64 bits.

1.8 Supporting structures

1.8.1 Serial Interconnect

In addition to the primary bus, there are additional communication systems on the backplane. These include a 10 Megabit Ethernet (10Base2), and lines reserved for IEEE 1394-1995 Firewire.

The Maintenance Bus also provides a very low speed interconnect between the boards and support equipment for the purpose of maintaining and testing the bus systems. This bus is an implementation of the IEEE 1149.5 MTM bus. This bus is described later in the chapter on the Maintenance Bus.

Ethernet provides communications between the boards in the system and through a hub located on the Central Service Module (CSM) to the outside world for a low cost connection between bus systems.

Firewire (IEEE 1394-1995) can provide read/write capability to the boards in the system when a redundant path is needed with a single main bus. Boards that use this system of redundancy would all need to support the 1394 interface. Firewire is a multimaster bus and can be used when more than one processor is available.

IEEE P2100 is added to the system through a bridge in one or more of the bus slots. As P2100 devices become available, the bridge may be added to the CSM function.

1.8.2 Support Signals

Support signals on the backplane include:

CCLK10M - 10.0000 MHz Constant Clock line (accuracy to be determined)
REQP0# - REQP3# - Bus Request Priority Request Pins.

CCLK10M, Constant clock line, has a frequency of 10.00 MHz and is used as a reference frequency. This frequency may also be used as the clock for the IEEE Std 1149.5 MTM maintenance bus. The bus clock in this system has a frequency range for 0 to 66.66Mhz and may use the 0 Hz for debugging, and power conservation functions, and can not be counted on as present for board level functions.

REQP0# - REQP3# are the request lines for the priority request system for the bus. These signals work in conjunction with the PCI REQ# signal and the FRAME and IRDY signals to establish 16 levels of bus request queing with round robin scheduling within each que and to prevent starvation at lower priority levels.

1.9 Electrical Specifications

Several different specification are used within this standard: 1) the LVTTL 3.3V signaling levels of the main PCI style parallel structure; 2) 3.3V PECL signaling for the TDM bus; 3) Ethernet ECL signal levels for the ethernet and 4) Firewire signal levels for the IEEE 1394-1995 bus.

1.9.1 Connector Pin Assignments

The first pinout shown in Table 3-? is for the normal bus module that connects to any position on

Table 3—Non-CSM Position Connector Pin Assignments

	a	b	c	d
1	P48VA	FGND	P48VA	P48VA
2	P48VA	FGND	N48VA	N48VA
3	N48VA	P48VAPRE	N48VA	ISHAREA
4	P48VB	N48VAPRE	P48VB	ISHAREB
5	P48VB	P48VBPRE	P48VB	N48VB
6	N48VB	N48VBPRE	N48VB	N48VB
7	ENET	GND	1394CLK	1394DATA
8	AD32	GND	AD33	SAD15
9	AD34	GND	AD35	AD36
10	AD37	GND	AD38	AD39
11	AD40	GND	AD41	SAD14
12	AD42	GND	AD43	AD44
13	AD45	GND	AD46	AD47
14	AD48	GND	AD49	SAD13
15	AD50	GND	AD51	AD52
16	AD53	GND	AD54	AD55

Table 3—Non-CSM Position Connector Pin Assignments

	a	b	c	d
17	AD56	GND	AD57	SAD12
18	AD58	GND	AD59	AD60
19	AD61	GND	AD62	AD63
20	PAR64	GND	C/BE4#	SAD11
21	C/BE5#	GND	C/BE6#	C/BE7#
22	ACK64#	GND	REQ64#	CCLK10M
23	AD00	GND	AD01	SAD10
24	AD02	GND	AD03	AD04
25	AD05	GND	AD06	AD07
26	C/BE0#	GND	M66EN	SAD09
27	AD08	GND	AD09	AD10
28	AD11	GND	AD12	AD13
29	AD14	GND	AD15	SAD08
30	C/BE1#	GND	PAR	SERR#
31	SBO#	GND	SDONE	PERR#
32	LOCK#	GND	STOP#	SAD07
33	IRDY#	GND	TRDY#	DEVSEL#
34	FRAME#	GND	C/BE2#	AD16
35	AD17	GND	AD18	SAD06
36	AD19	GND	AD20	AD21
37	AD22	GND	AD23	IDSEL
38	C/BE3#	GND	AD24	SAD05
39	AD25	GND	AD26	AD27
40	AD28	GND	AD29	AD30
41	REQ#	GND	AD31	SAD04
42	SAD03	GND	TX+	RX+
43	GNT#	GND	TX-	RX-
44	SAD01	GND	MCLK	SAD02
45	CLK	GND	REQP0#	SAD00
46	REQP1#	GND	REQP2#	RST#
47	MMD	GND	MSD	REQP3#
48	MPR	GND	MCTL	Spare5#
49	user defined	user defined	user defined	user defined
50	user defined	user defined	user defined	user defined
51	user defined	user defined	user defined	user defined
52	user defined	user defined	user defined	user defined
53	user defined	user defined	user defined	user defined
54	user defined	user defined	user defined	user defined

the bus other than for the CSM module position, the use of rows 49 to 54 are define by the board and connect through on the backplane to provide user I/O with a flexible connection

Central Service modules require the additional pins to provide the clocks and arbitration for the bus

Table 4—CSM POSITION CONNECTOR Additions

	a	b	c	d
48				BPSN#
49	CLKS0	CLKS6	REQ0#	GNT0#
50	CLKS1	GNT6#	REQ1#	GNT1#
51	CLKS2	REQ6#	REQ2#	GNT2#
52	CLKS3	GND	REQ3#	GNT3#
53	CLKS4	PUPOWER	REQ4#	GNT4#
54	CLKS5	PUPOWER	REQ5#	GNT5#

segment of up to 8 slots. The above chart shows the changed definitions for a 7 slot backplane entity.

On 12su boards an additional set of 72 pins are located in the center of the board and are defined for the TDM bus and the service modules clocks for the TDM bus and the REDUNDANT TDM structure. The pinouts for this connector are:below.

Table 5—CSM Connector

	a	b	c	d
1	ATDM0	GND	ATDM1	ATDM2
2	ATDM3	+1.3VTTA	ATDM4	ATDM5
3	ATDM6	GND	ATDM7	ATDM8
4	ATDM9	ATDM12	ATDM10	ATDM11
5	ATCLK6+(in)	ATCLK6+(out)	ATDM13	ATDM14
6	ATCLK6-(in)	ATCLK6-(out)	AFRAME	ATDM15
7	ATCLK0+(out)	ATCLK1+(out)	BTCLK0+(out)	BTCLK1+(out)
8	ATCLK0-(out)	ATCLK1-(out)	BTCLK0-(out)	BTCLK1-(out)
9	ATCLK2+(out)	ATCLK3+(out)	BTCLK2+(out)	BTCLK3+(out)
10	ATCLK2-(out)	ATCLK3-(out)	BTCLK2-(out)	BTCLK3-(out)
11	ATCLK4+(out)	ATCLK5+(out)	BTCLK4+(out)	BTCLK5+(out)
12	ATCLK4-(out)	ATCLK5-(out)	BTCLK4-(out)	BTCLK5-(out)
13	BTDM0	GND	BTDM1	BTDM2
14	BTDM3	+1.3VTTB	BTDM4	BTDM5
15	BTDM6	GND	BTDM7	BTDM8
16	BTDM9	BTDM12	BTDM10	BTDM11
17	BTCLK6+(in)	BTCLK6+(out)	BTDM13	BTDM14
18	BTCLK6-(in)	BTCLK6+(out)	BFRAME	BTDM15

The second set is for the normal board case of not being in the CSM position. This connector is

	a	b	c	d
1	ATDM0	GND	ATDM1	ATDM2
2	ATDM3	NC	ATDM4	ATDM5
3	ATDM6	GND	ATDM7	ATDM8
4	ATDM9	ATDM12	ATDM10	ATDM11
5	ATCLK6+(in)	NC	ATDM13	ATDM14
6	ATCLK6-(in)	NC	AFRAME	ATDM15
7	user-defined	user-defined	user-defined	user-defined
8	user-defined	user-defined	user-defined	user-defined

	a	b	c	d
9	user-defined	user-defined	user-defined	user-defined
10	user-defined	user-defined	user-defined	user-defined
11	user-defined	user-defined	user-defined	user-defined
12	user-defined	user-defined	user-defined	user-defined
13	BTDM0	GND	BTDM1	BTDM2
14	BTDM3	NC	BTDM4	BTDM5
15	BTDM6	GND	BTDM7	BTDM8
16	BTDM9	BTDM12	BTDM10	BTDM11
17	BTCLK+(in)	NC	BTDM13	BTDM14
18	BTCLK-(in)	NC	BFRAME	BTDM15

shown below. Additional configuration options are under consideration that will allow for more rear I/O from the board. Within the 24pin blocks additional configurations are available the include single RF or Fiber I/O and up to 6 RF/Fiber connectors per block using smaller diameter coax/fiber. These configurations include:

1. 6su board with only 32 bits of address and data (opens up about 36 I/O lines)
2. 12su board with out redundant bus or TDM (frees middle connectors and lower connectors.
3. 6su and 12su boards with mechanical keying to support the use of Fiber and RF connectors.
4. 18su and 24su boards with additional sets of connectors.

Part of the effort here is to prevent these boards from plugging into destructive conditions. For this purpose the board that have RF or Optical connectors in place of the normal pin I/O will have connectors keyed to prevent the insertion of the normal pin I/O into the backplane positions with the RF/OPTICAL connectors

1.9.2 Power Distribution

The power paradigm for this system is the distribution of redundant wide tolerance main voltage with local voltage regulation as needed. The distribution power rails are DC isolated from the incoming power supply to meet isolation requirements of 3750V with required creepage and clearances distances. It is also expected that the onboard regulators will also be DC isolated from the power rails with the only common element from node to node being signal ground.

This power is distributed through dual power rails, each rail can deliver up to 4 Amps of power at a nominal voltage of 48V to each board slot. This nominal 48V supply has a range of 36V to 58V. This stays within the definitions of “Safety Extra Low Voltage” that will comply with IEC 950 and EN 60 950 for European requirements and UL1450 for US requirements. This voltage provides sufficient power while reducing the current density in the connector pins. In telecommunication system the voltage would be a nominal 52.8V to 55V with normal batteries under charging conditions.

Additional precharge lines are located on longer pins to bring the input circuits up to voltage before the main power pins connect. The precharge pins are current limited to 100 mA for safety on the long pins. The last pins to make contact on each set of power rails is the power-on pins to start the onboard power converters.

Power rail A contain 11 pin:

Power rail B contain 11 pin:

The remaining two pins in the first block of 24 pins are FGND = Frame Ground. This ground is used on a strip around the board and contacts the grounding clips on the card guides. Frame Ground is isolated from common signal ground. Overall the power block of 24 pins looks like this:

Table 6—A Power Rails

Positive Rail	Negative Rail	Voltage Difference	Maximum Current	Number of pins
P48VA	N48VA	36VDC to 58VDC	4 Amperes	4 pins per Rail
P48VAPRE	N48VAPRE	36VDC to 58VDC	0.1 Ampere	1 pin per Rail
ISHAREA	N48VA	0 to 15VDC	20 mA	1 pin

Table 7—B Power Rails

Positive Rail	Negative Rail	Voltage Difference	Maximum Current	Number of Pins
P48VB	N48VB	36VDC to 58VDC	4 Amperes	4 pins per Rail
P48VBPRE	N48VBPRE	36VDC to 58VDC	0.1 Ampere	1 pin per Rail
ISHAREB	N48VB	0 to 15VDC	20 mA	1 pin

Table 8—Power Pin Locations on connectors

Row\Column	a	b	c	d
1	P48VA	FGND	P48VA	P48VA
2	P48VA	FGND	N48VA	N48VA
3	N48VA	P48VAPRE	N48VA	ISHAREA
4	P48VB	N48VAPRE	P48VB	ISHAREB
5	P48VB	P48VBPRE	P48VB	N48VB
6	N48VB	N48VBPRE	N48VB	N48VB
Length	**6.5 mm**	**8 mm**	**6.5 mm**	**5.75 mm**

1.10 Mechanical Specifications

1.10.1 Mechanical Sizes

This standard uses the Hard Metric mechanical system with the following features:

- IEC 917-2-2/IEEE Std 1301-1992 standard dimensions
- Board top surface offset 10 mm from left reference on module (from the front panel)
- Board position allows front and back component placement (7.23mm back, 19mm front)
- 30 mm front panel allows 1 inch disk drives on boards

1.10.1.1 HiRelPCI Connectors

- 2mm Connectors - FutureBus style - Metral style
  - Bellcore, UL, CSA approved
  - IEC 1076-4-OX (48B) compliant
  - EIA 616 compliant
  - Stackable connectors for I/O

8x24 short pin = Berg Part Number 70235-977 or equivalent
1x24 short pin = Berg Part Number 70232-977 or equivalent
1x24 Long pin for rear plug = Berg Part Number 70232-987 or equivalent
Standard RF and Optical I/O available for I/O connector positions
Keying available to prevent damage when mixing RF and pin I/O
Staggered Pin Height to support Live Insertion
A Row = 6.5mm
B Row = 8.0mm
C Row = 6.5mm
D Row = 5.75mm
Signal return path for every 2 signals.
6su boards contain
216 pins - 4 column of 54 pins including 24 user defined I/O pins
12su boards contain
504 pins - 4 columns of 126 pins including 72 user defined I/O pins and TDM blocks

1.10.1.2 HiRelPCI board formats

6su HiRelPCI
6su = 115mm (4.53") x 213mm depth (8.39")
12su HiRelPCI
12su = 265mm (10.43") x 288mm depth (11.34")

1.10.1.3 HiRelPCI board size comparison to VME style boards

6su HiRelPCI ~ 3u VME style
Board Size -115mm x 213mm vs. 100mm x 160mm
Board Area - 245 sq. cm vs. 160 sq. cm raw size
Usable Area - 430 sq. cm vs. 140 sq. cm component area
12su HiRelPCI ~ 6u VME style
Board Size - 265mm x 288mm vs. 233.35mm x 160mm
Board Area - 763 sq. cm vs. 374 sq. cm raw size
Usable Area - 1416 sq. cm vs. 336 sq. cm component area

1.10.2 Environmental

P1996 is intended to operate in the following environmental conditions:
Temperature -40C to +85C
Humidity 0 to 100%
Altitude -100m to +15000m
Cooling
Convection cooling for transportation and other severe environmental applications.
Forced air cooling may be used in telecom and other less demanding environmental applications.

1.11 IEEE PAR TITLE

Standard for an Extendible High Reliability Enhanced PCI Bus

1.12 IEEE PAR PURPOSE of P1996 HiRelPCI

Purpose: The transportation, telecommunications, and process control industries need reliable high availability fault tolerant systems that support harsh environments and extended temperature ranges, with packet protocols that support serial interconnections to similar systems at speeds from 10 megabits/sec to >1 gigabit/second. There is no currently defined standard for such systems that can take advantage of the enormous (and still growing) industrial support for the PCI system by way of silicon, software, and tools. This standard is intended to fill that need.

1.13 IEEE PAR SCOPE of P1996 HiRelPCI

Scope: This project will develop a Standard for an Extendible High Reliability Enhanced PCI Bus for transportation, telecommunications, and process control systems. This bus will define and use PCI-style protocol, extending it to include packet messages as defined in the SCI(IEEEstd 1596-1992) and Serial Express (P2100) projects. This bus will include redundancy and support hot swap of boards for fault tolerant, high availability operation. This project will include the physical and electrical implementation of this bus and define the interface to a high speed serial interconnect such as the Serial Express bus. For telecommunication applications, an optional Time Division Multiplexed bus using international signaling rates from the Synchronous Digital Hierarchy will be defined.