P1996: High Reliability and Extensibility with PCI and SCI

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0.1 The Need

This bus came from a need to provide a High Reliability, High Availability system for transportation control and telecommunications systems. Transportation and traffic control have a need for very low system failure rate in difficult environments. These system must operate on the street corners from northern Alaska to the southern deserts of Arizona with the extremes of temperature and humidity prevalent. The telecommunications requirements are not quite as severe in the environmental area, but are similar in the need for R.A.M. (Reliability, Availability and Maintainability) plus the additional need of a Time Division Multiplexed bus for circuit switched data using elements of the international Synchronous Digital Hierarchy (SDH) at rates defined in ANSI T1.105-1991. Both areas of usage need redundant capabilities to allow continued operation with a single fault. Additional areas of interest for this project are Process Control, Communications, and embedded systems.

Continuous Service and Extensibility are the key components that make this effort somewhat different from other busses that exist.

0.1.1 Continuous Service

A goal of high reliability/high availability system is that the system provides for Continuous Service. Such a system may degrade, with the loss of a resource, but may not cease to function at the failure of any given resource. This in turn implies that there is no single point of failure in the system. This has been tackled with the following redundant elements;

- Redundant Elements including
  - Buses
  - Power
  - Resources
- Flexible Configuration
- Protection from rogue elements
- Distributed Configuration Control
  - Resource Mapping and Management
- Multiple Access Methods
  - Mapping controls to CSR Address Space
  - Access via PacketBus
  - Access via PCI
  - Access via MTM bus
  - Access via Backplane serial busses

New requirements addressed in this work are primarily directed to the extending the capabilities of exisiting element to meet the above needs.

These elements are designed to meet the needs of mission critical computers.

0.1.2 Extensibility

These application areas need a method of extending beyond the local bus to other similar buses in a uniform, redundant manner. The solution to this need was to include a provision in the bus to handle the message packets of the IEEE Std 1394-1995, P1394.2 (formerly Serial Express) and IEEE Std 1596-1992 SCI. This addition provides for 64K addressable nodes and a uniform 64 bit address space. In more demanding multiprocessor systems, the cache coherency methods of SCI can be employed as needed.

0.1.2.1 System Configurations

- Small System 2 - 8 nodes 1 level interconnect
  - Serial Express Interconnect
  - PacketBus Interconnect
  - SCI Interconnect
- Medium System 4 - 64 nodes 2 level interconnect
  - Serial Express Interconnect 3 - 4 Busses
  - PacketBus / Serial Express Interconnect
  - SE/PacketBus/SCI Interconnect
- Medium System 4 - 64 nodes Redundant Links
  - Serial Express Interconnect 3 - 8 Busses
  - PacketBus / Serial Express Interconnect
  - SE/PacketBus/SCI Interconnect
  - Multiple Servers - Multiple Disk arrays
- Large System 20 - 4096 Chassis 20 - 64K nodes Multiple Redundant Links
  - Serial Express Interconnect 3 - 100+ Busses
  - PacketBus / Serial Express Interconnects
  - SE/PacketBus/SCI Interconnect
  - 2 to 4 links / PacketBus
  - Different types of links

These systems are needed for:

- Continuous Operation Systems - Multiple Nodes Multiple Crates
  - Traffic Control, Air and Ground
  - Telephony
  - (medical)
  - Security
  - Safety systems

In these system NO SYSTEM WIDE RESETS can be allowed.

This bus is designed to satisfy these needs.

0.1.3 FEATURES OF THIS HiRelPCI BUS

The following set of features of the P1996 HiRelPCI Bus drive its utility:

- Reliability - Through passive backplane, Redundant Buses, Redundant power
- Availability - Through design for NO Single Point of Failure
- Maintainability - Through MTM bus, Hot Swap, Standby modules
- Scalability - Through PacketBus to P1394.2 and SCI, Circuit Switch I/O through STS-12
- Performance - PacketBus performance to 533 MByte/second with up to 95.5% efficiency
- Redundancy - no single point of failure on a normally configured system.
- -40C to +85C Industrial/Automotive temperature range operation
- Power Distribution at nominal 48V for efficiency
- Configuration Management through CSR Architecture, Serial Express and MTM busses
- Redundant connectivity through backplane Firewire and 10B2 ethernet

0.2 ELEMENTS OF HiRelPCI BUS

This bus standard is a combination of elements taken from other standards and modified to provide the structure to meet the needs described above. The elements that make up this high reliability, high availability bus include:

1. A Parallel system bus using PCI style signaling for normal bus access
2. A PacketBus added on top of the Parallel system bus for packet switched connections
3. A Time Domain Multiplexed bus for circuit switched connections
4. A maintenance bus for control of system resources for hot swap operations
5. An Addressing structure that uses the larger 64 bit address space
6. Several supporting interconnection systems
7. A set of electrical specification for low voltage signaling, GTL+ signaling and power
8. A set of mechanical specifications to provide a well defined enclosure system

The combination of these elements build a system that provides:

1. Extensibility to 64K nodes of 256 Terabytes each
2. IEEE 1212-1991 CSR Architecture for easy expansion via SCI, Serial Express,1394-1995 etc.
3. Redundant functions to provide no single point of failure for continuous operation
4. Hot Plug of any board to replace faulty modules or update features.
5. Circuit Switched base for Audio, Telephony, Video, ATM for consistent external/internal model
6. Packet Switched connection model for shared memory operations via SCI/SE internal and external

0.3 Bus Signal Definitions

Nominal bus signaling on the P1996 is based on the PCI Local Bus Specification 2.1 using 3.3V signal levels. This provides leverage on all the silicon built to support the PCI market. This protocol is flexible and provides performance from 0 - 533 megabytes per second, read and write burst transactions.

This bus has been extended to include a packet mode, called PacketBus, to support the packets sent over the SCI/Serial Express busses to extend transparent communications, through common memory mapped access, to other elements of a distributed, redundant system. Packet operations are transparent to the normal PCI transactions compliant to Rev 2.1. HiRelPCI bus can operate in PacketBus, normal PCI mode or a mix of both modes. PacketBus mode of operation can be used to expand the normal PCI functions and will be proposed to the PCI technical committee for inclusion in the future PCI Local Bus specifications.

PacketBus is possible by the addition of a command mode on the PCI that is a write only mode. Write Only operations are supported in both 32 and 64 bit wide operations that will deliver the bit serial equivalent of 4.266 gigabits per second.

Today’s limitation on the driver technology, as limited by the extreme cost effective considerations of the motherboard environment, and the physics of the backplane restrict the number of backplane segment positions to 7, or 8 when stretched. Extensibility is required to extend the operation to additional nodes in systems attached through SCI/Serial Express links.

Each component in the system is attached to the Maintenance Bus which is a bus defined by the IEEE Std 1149.5-1995 documents. Maintenance Bus signal lines are shown in Table 1

Table 1—Maintenance Bus Signals

Signal Name	Signal Function	Signal Direction
MCLK	MTM Clock	To all from CSM
MMD	Master Data	From Master
MSD	Slave Data	To Master
MPR	Master Pause Request	To Master
MCTL	Master Control	From Master

0.4 Parallel Bus Operations

In addition to the normal PCI style operation, additions and deletions have been made to improve the operation of the bus. Specific additions have been the prioritized bus request facilities, PacketBus, and the MTM maintenance bus and 48VDC power, constant clock, backplane 10Base2 ethernet and Firewire. Specific deletions are INTB#, INTC# and INTD#, 5VDC and 3.3VDC power.

0.4.1 CSM Functions

Centralized resources needed for bus operations are supplied by the Central Services Module. There shall be at least one CSM attached to each bus segment. In most cases, a CSM will span two HiRelPCI buses in the 12su configurations and only one bus in the 6su configuration. This module provides all the clocking and arbitration for the parallel bus and the TDM bus when present.

The Central Services Module provides the following services for the bus:

- Clock drivers for each slot on the bus segment
- Bus Arbitration for each slot on the bus segment
- Repeater Hub for the Ethernet signals
- Repeater Hub for the 1394 Firewire serial bus
- Possible location for Bridge to IEEE P1394.2
- PCI to PCI Bridge if needed
- Possible TDM interface between outside world and backplane bus
- TDM to TDM Bridge and framing store if needed
- Clocks for the TDM slots when used
- System monitor functions
- Maintenance Bus Master

0.4.2 Priority Bus Request Mechanism

This provides a prioritized request in addition to the normal round robin Fairness priority system of the PCI bus. This priority scheme uses four pins REQP0# to REQP3# to define the priority level of each bus request as level 0 to 15. Bus request are issued at the rising edge of FRAME# by activating their REQ# and priority level on REQP[3::0]#. The priority level on the bus for this cycle is seen by all participants. Lower level requesters will retire and remove the REQ# if a higher level request is pending. The CSM arbiter determines the winner or winners and issues the bus grants to the boards with the highest level of priority on a round robin basis and then to the next lower level of priority on a round robin basis until there are no pending bus requests.

Prioritized bus requests may have 1 to 8 requests pending at any given level of request, the requests are granted in round robin priority until all are issued while building a queue at the same level to insure fairness within the bus request queueing level. This also guarantees priority among the bus request queueing levels.

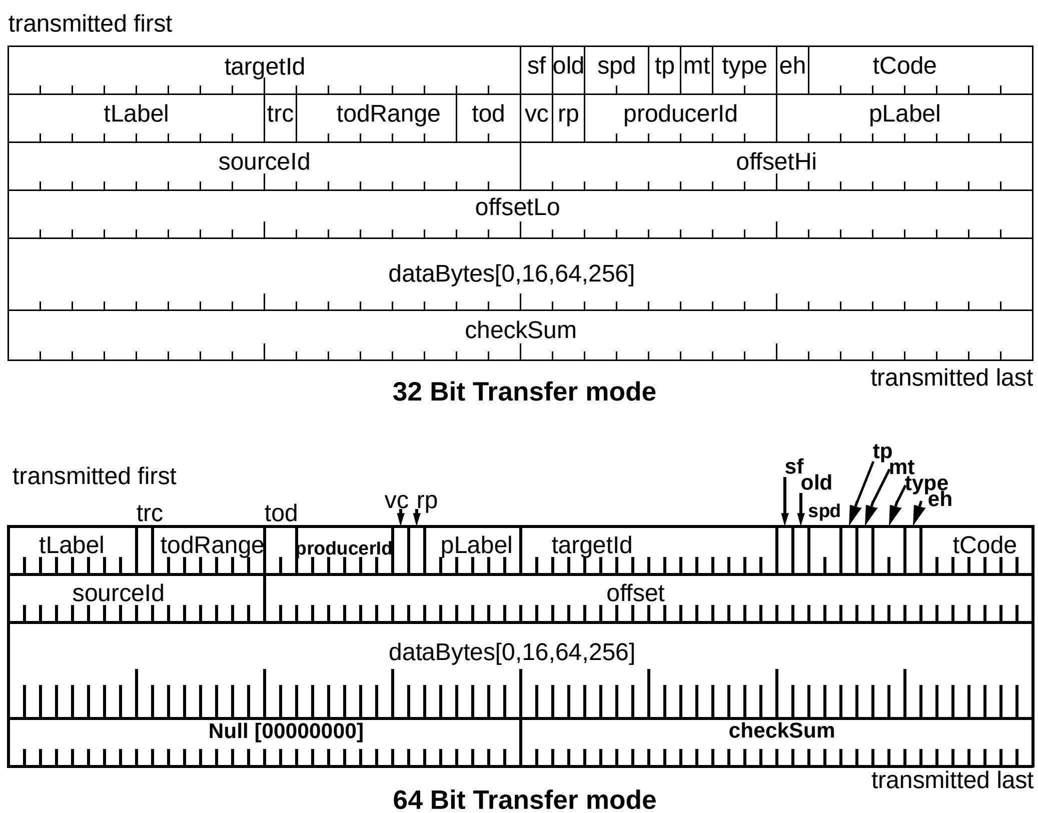
Boards using the PCI style single REQ# line will request at bus request level 0. Any higher level of request will block the lower level request. This mechanism is transparent to the single level request mechanism and will be seen as a probably longer delay until a GNT# is received.

0.5 PacketBus Operations

PacketBus operations are added to the basic parallel bus structure to improve the performance of the system with a split response mode of operation and as the bridge to the larger system in the common memory mapped architecture. This mode is also known as a write only mode of bus operation in that each request and response is a separate write transaction. The basic function is to free the bus resource during the time needed to fetch or process the data at the target end of the transaction. Packet mode operation does impose additional requirements on the participants as buffers are needed to handle the packets queueing to and from the bus.

PacketBus operation is optional for the HiRelPCI bus. This mode can be used to produce the highest bandwidth operations on the bus with greater than 4 gigabit throughput feasible. With the minimum data transfer of 16 bytes the efficiency of the bus is about 40%, the larger data packets up to 256 bytes have increasing efficiency up to 95.5%.

PacketBus operations require the use of a new command mode in the PCI specification and the redefinition



Send/Request Packet

of several of the PCI signal lines during this mode of operation. In all cases these changes are transparent to the existing PCI devices.

The preferred command mode is the “0101” mode which would be an unused WRITE transaction. Current devices are required by PCI Local Bus Specification Revision 2.1 to ignore this command code and hence no interference with the existing operations. These packets are of the general form shown in Figure 1 below.

A command field identifies the different forms of send packets, as illustrated in drawing above.

0.5.1 CSR Space Mapping and Configuration Operations

All operations and accesses are through a common memory mapped system space. At each node on the system there is a CSR space. Through this CSR space and its map, access to the elements is controlled. The MTM bus, the PCI Configuration Space, and the CSR registers are all available mapped into this single space. The flexibility of the system depends on this mapping.

0.5.2 Node Addressing

Extending beyond a single PCI style bus is required for applications that need more or vastly more processors, memory and I/O boards. Redundant operations also require more than one processor, memory and I/O board. Connectivity beyond a single system is greatly enhanced by addressing a card slot on a bus segment as a node. Each slot has a node address consisting of 16 bits, split into 3/4 bits of slot-id and 12/13 bits of address assigned by a jumper on the backplane or by a bridge to the SCI/P1394.2 node address. This allows up to 4092 bus segments of 16 slots/nodes each. P1394.2 bus addressing which is defined around 1024 buses of 64 nodes each and makes specific allowances to support more busses of less nodes. All addressing for normal operation is directed to 16 bit nodeId which are routed to the proper node.

These 16 SAD pins are distributed along the connector and AC bypassed to ground, or connected to ground to provide a high quality signal return path.

On 12su dual bus systems, the SAD lines on the top connector are used for identification and the bottoms SAD lines are made a duplicate of the top lines for redundant operations.

IEEE 1212-1991 addressing is used with these 16 bits defining a slot as one of the 65536 in the address space. Each node has a sub address range of 48 bits for total address space of 64 bits.

0.5.3 Requirements

0.5.3.1 Extensibility

Over all system must be able to grow uniformly from a small system of two of three nodes to a full grown system that approaches the maximum possible configuration of 64K nodes on 4096 to 8192 smaller busses.

Reset and Restart operations need to be defined on the smallest segment space possible. This is to prevent undesirable global resets.

0.5.3.2 Start-up

The system must be able to start-up cleanly in small (1 node) to largest (64k nodes) and in deterministic order. Start-up and reconfiguration shall be completed by any node in the system. This implies and requires that the MTM bus must be addressable through the external link from within or outside of the current set of nodes once a link has been established to other nodes.

0.5.3.3 Uniqueness

After Start-up and system configuration, the elements of the system must have unique identifier. This identifier must be available for identification and correlation to the soft nodeId.

Hot Swap Support - each node/system must be able to turnoff and unplug a broken board and replace with a new board without complete reconfiguration of the system. In some cases the softId can be transferred to the replacement unit if that unit duplicates the unit being replaced functionally.

Hot Standby Support - Redundant equipment in standby partial power mode. These modules can be activated to replace a failed resource.

Multiple Links on Nodes - Each PacketBus may/must have multiple links for redundancy - TBD - How are addresses assigned and what happens when another link is added?

EUI - Extended Unique Identifier - A 64 bit number that is unique as an identifier of this particular component.

Company ID - A 24 bit numerical identifier for a company that is assigned by the IEEE Registration Authority Committee. This number identifies the company that made the equipment.

NodeId - The 16 bit address that is the upper 16 bits of the 64 bit address. This address determines the target of a packet or the strip address of a broadcast packet in a ring structure.

Soft addresses/softId - This is the address assigned to a node or set of nodes following the configuration of the extended system.

Hard addresses - Initial address before Links are working and have negotiated a unique set of addresses.

Multicast Addresses - A packet address directed to group of functions.

Broadcast Addresses - A packet address that targets all groups of targets

Domain - Addresses within a 14-16 slot chassis

Resource Map - Refer to the Resource map definition section below.

0.5.4 Resource Map definition

Overall structure of this map is shown in Table 2. This resource map defines the association between the assigned resourceId and the EUI and other address used to access this single element/node. The location of the map is stored in the CSR register set with an offset of 3CO and is 8 bytes long. This will point to any location within the available memory of the system. The secondary pointer is located at 3C8 and is used if the primary map is corrupted. Individual resource contents of the map are shown in Table 3.

Entries in the overall map shown in Table 2 are:

1. Map overall length in bytes: This length is used to determine the space required for the table.
2. Name of Table: This is used to distinguish between the several tables that are kept for redundancy purposes. The specific method of naming the table is TBD.
3. Configuration: This element defines the configuration of the table from basic 2 entry table to full table that contains the extended information about the node and the security for the node.
4. First entry offset: This is the offset from the beginning of the table to the location of the first resource entry.
5. Authentication: This element of the table is the authentication of the table. This is defined by the last modification of the table and the nodeId of the configuration node and possibly a signature of the configuration node.
6. Checksum; Over all 32 bit checksum for all entries in the table.

Table 2—Resource Map Table

Offset address	Length	Description
0	4	Table length in bytes
4	2	Map Name
6	2	Map Configuration node
8	2	Offset to 1st entry
A	6	Reserved
10	16 - 32	Map authentication
length - 4	4	Map checksum

Table 3—System Resource Map Entry

Offset	length	Description
0	2 bytes	SoftId
2	2	Entry length and map
4	4	reserved.
8	8	Extended Unique Identifer
10	2	Configuration Node
12	2	Configuration signature
	n	Multicast/Broadcast pools
	16 - 32	Resv’d node public key
	4	checksum

Entries for Resource map shown in Table 3 are;

1. SoftId: Assigned softId for the node. This is used to index into the table.
2. Entry length and map: Length of this entry and map number.
3. Reserved: Reserved for alignment reasons for the EUI to start on an 8 byte boundary.
4. EUI: Extended Unique Identifier for Node from the EUI attached to board.
5. Configuration Node: Node number of the node that configured this board.
6. Configuration Signature: Signature of the configuring node
7. Multicast/Broadcast Pool: This list is 2 byte (16bit) softId identifiers used in multicast and broadcast operations on this resource. This may contain 0 or more entries.
8. Reserved for node publickey signature: For more secure environments, This public key plus the private key maintained on the board, authenticate operation and changes to the setup of the board.
9. Entry Checksum: Checksum for this entry in the table.

0.5.5 Addressing

This standard adheres to the IEEE Std 1212-1992 Control and Status Register Architecture standard using the 64 bit fixed address model. This architecture is fundamental to the operation of the extensible system. No other architecture can provide the shared memory, coherent, memory system that smoothly grows for a single processor to 65K+ nodes (processors, memory, storage resources, DSP resources, system communication nodes) for the growth into the future of your system. Each node has the same registers in the same address location which permits the management of large system

Within HiRelPCI, hot plugable boards, many of which will be of similar design, geographical addressing is used to guarantee that each node in the system has a unique node address. Different geometries will have different needs depending on the type of chassis and the extent of subsystems within the chassis. It is the responsibility of the system designer to insure that each board that is plugged into a backplane will have a unique address for the A(63::48) nodeId address domain.

For descriptive purposes we will assume that there are up to 8 nodes on a given backplane bus segment and that 2 segments are joined for a possible total of 16 addressable elements in a given chassis.

Of the 64 Bit address A(63::48), the nodeId address shall be unique to the board. Other nodeId’s may be assigned by software to form multicast and broadcast addresses. For our example A(51::48) provides the Geographical Address within the bus to guarantee uniqueness on the bus with a start-up hardId address and unit addresses, if not reconfigured by external software agents.

If a backplane were to include four independent PCI segments then A52 is used to differentiate top bus from bottom bus.

Configuration software, after initialization, will use A(63::52) to determine chassis identity and then A(47::0) will determine the Addressing within that node.

Within the node the address is initially defined in the CSR (IEEE Std 1212 - 1992) as shown in Table 4:

Table 4—Basic 64 Bit Fixed Address CSR Architecture

Begin Address nnnn = nodeId	End Address nnnn = nodeId	Function
nnnn 0000 0000 0000	nnnn 0000 0FFF FFFF	Register Address Space
nnnn 0000 1000 0000	nnnn 0000 1FFF FFFF	Node Private Address Space (256M)
nnnn 0000 0000 0000	nnnn 0000 0FFF F7FF	Initial Units Address Space (256M-2K)
nnnn 0000 0FFF F800	nnnn 0000 0FFF FFFF	Initial Register Address Space (2K)
nnnn 0000 2000 0000	nnnn FFFF FFFF FFFF	Initial Memory Space (281 Tbytes- 2^{40})

0.5.6 P1996 CSR Register Definitions

The CSR registers are at fixed addresses offset relative to *nnnn 0000 0FFF* $F800_{16}$ as shown in Table 5 where nnnn is the 16 bit address of the node.

The CSR Architecture defines registers that are 4 bytes (or larger) in size. To ensure interoperability across bus standards, the ordering of the bytes within these registers is defined by their relative addresses, not their physical position on the bus. Bus bridges are similarly expected to route data bytes from one bus to another based on their addresses, not their physical position on a bus. The routing of data bytes based on their address is called address-invariant. Within the HiRelPCI bus operations in the PCI domain, the bytes are transferred to the PCI ordering. External references reorder the bytes to support the address-invariant format. For a quadlet CSR access, the data byte with the smallest address is the most significant.

Table 5—CSR Register Space Address Allocations

Offset into CSR REGS	Offset in Hex nnnn 0000 0FFF F800	Register Name	Required
	0	STATE_ CLEAR	
	4	STATE_ SET	
	8	NODE_IDS	Required
	C	RESET_START	Required
	10	INDIRECT_ADDRESS	
	14	INDIRECT_DATA	
	18	SPLIT_TIMEOUT_HI	
	1C	SPLIT_TIMEOUT_LO	
	20	ARGUMENT_HI	
	24	ARGUMENT_LO	
	28	TEST_START	
	2C	TEST_STATUS	
	30 - 4C	Reserved for Extended Memory Space	
	50	INTERRUPT_TARGET	
	54	INTERRUPT_MASK	
	58	CLOCK_VALUE_HI	
	5C	CLOCK_VALUE_MID	
	60	CLOCK_TICK_PERIOD_MID	
	64	CLOCK_TICK_PERIOD_LO	
	68	CLOCK_STROBE_ARRIVED_HI	
	6C	CLOCK_STROBE_ARRIVED_MID	
	70 -7C	CLOCK_INFO(0-3)	
	80 - BC	MESSAGE_REQUEST	
	C0 - FC	MESSAGE_RESPONSE	
	100 -180	Reserved	
	180 - 1FC	ERROR_LOG_BUFFER	
	200	PCI DeviceID VendorID Register 00h	Required
	204	PCI STATUS COMMAND Register 04h	Required
	208	PCI ClassCode RevisionID Register 08h	Required
	20C	PCI INFO Register 0Ch	Required
	210	PCI Base_Address_0 Register 10h	
	214	PCI Base_Address_1 Register 14h	
	218	PCI Base_Address_2 Register 18h	
	21C	PCI Base_Address_3 Register 1Ch	
	220	PCI Base_Address_4 Register 20h	
	224	PCI Base_Address_5 Register 24h	
	228	PCI CardBus CIS Pointer Register 28h	
	22C	PCI SubSystemID SubSystem VendorID 2Ch	
	230	PCI Expansion ROM Base Address Register 30h	
	234	PCI Reserved Register 34h	
	238	PCI Reserved Register 38h	
	23C	PCI Grant Interrupt Info 3c	
	240 - 2FC	PCI REGISTER EXPANSION	
	300 - 307	MTM Fault Logs	Required
	308 - 30F	MTM Test Data Storage	
	310	MTM Slave Status Register	Required

Table 5—CSR Register Space Address Allocations

Offset into CSR REGS	Offset in Hex nnnn 0000 0FFF F800	Register Name	Required
	314	MTM Bus Error Registers	Required
	318	MTM Module Status Register	Required
	31C	MTM Additional Status Registers	
	320	MTM Manufacturers ID Port	Required
	324	MTM Module Manufacturer Port	Required
	328 - 32F	MTM User Identification Ports	Required
	330 - 34F	MTM Access to IEEE Std 1149.1 bus	Required
	350	MTM Command Register	
	354 - 35B	MTM Command Data Pointer	
	380 - 3BF	Voltage/Current/Temperature Storage	
	3C0 - 3C7	Pointer to Primary Resource Table	
	3C8 - 3CF	Pointer to Secondary Resource Table	
	3D0 - 3D7	Pointer to Primary Configuration Manager	
	3D8 - 3DF	Pointer to Secondary Configuration Manager	
	3E0 - 3FF	Reserved	
	400 - 7FC	ROM_WINDOW	Required

0.6 TDM Bus Operations

Dual TDM busses are included as an option for telecommunications and for ATM usage. ATM operation is defined as part of the SONET specification and the pointers required for its operation are allocated in the overhead region of SONET frame. The physical implementation of these busses share a common clock and frame signal. Each TDM block consists of 6 ground pins, 1 clock pin, 1 frame pin and 2 sets of 8 data lines. The clock pin is routed individually to each slot to provide tight timing specification.

This bus will follow the structure of ANSI T1.105-1991 SONET (as revised) using the blocking factors in the international standard. This standard provides a reference for multiple embedded carriers and provides an internationally accepted framework for circuit presentation and ATM integration if needed. Basic timing is provided by the CSM board position and consists of clocks with less than 1 ns of skew and a framing pulse to define the local chassis time slot count. Adjustment may be made to synchronize with one external source of framing information. The first 24 time slots are used for synchronization purposes and are used in this standard to move the relative frame time on different parts of the system to be in coordination with the back-plane requirements though frame buffers and other necessary techniques.

The overhead portions of the ANSI SONET standard are fully specified in the ANSI T1.105 1991 standard and are not modified in this usage. All Overhead bytes are passed through for use in downstream processing.

Worse case simulations, for voltage, process, and temperature, indicate clock speeds to 77.76 MHz using GTL+ logic to provide an upper limit of STS12 on each of the sets of data lines with positive timing margins.

12su systems would have dual TDM blocks for reliable redundant operation. Each of these busses has 2 byte wide paths that may be used as input and output streams and are each readable and writable on each time period. Each cycle is 12.86 ns in duration which requires terminated GTL+ bus to reduce reflections and lower the propagation delay to incident wave travel as the TDM bus is fully terminated.

0.7 Maintenance Bus Operations

The Maintenance Bus Master issues sets of commands that are fully described in the IEEE Std 1149.5-1995. These commands are summarized in the following table.

In addition to the normal commands provided by the 1149.5 command set, the command extension

Table 6—Maintenance Bus Commands

Command Class	Command Code (Binary)	Command Code (HEX)	Command	Status
Core	0000000	00	Read Status	Required
	0000001	01	Abort	Required
	0000010	02	Reset Slave Status	Required
	0000011	03	Contend for Bus	Required
	00001XX	04-07	Multicast Group Select	Required
	0001000	08	Enable Idle Interrupts	Required
	0001001	09	Enable Pause Interrupts	Required
	0001010	0A	Disable Idle Interrupts	Required
	0001011	0B	Disable Pause Interrupts	Required
	0001100	0C	Enable Module Control	Required
	0001101	0D	Data Echo Test	Required
	0001110	0E	Verify BMR	Required
	0001111	0F	Initialize Application	Required
	0010000	10	Disable Module Control	Required
	0010001	11	Start	Required
	0010010-0011111	12-1F	Reserved	Reserved
	1111111	7F	Illegal Command	Required
Data Transfer	0100000	20	Read Data	Recommended
	0100001	21	Write Data	Recommended
	0100010	22	Read/Write Data	Recommended
	0100011-010111	23-27	Reserved	Reserved
Module Initialization and Self-Test(MIST)	0101000	28	Reset Module with SBIT	Recommended
	0101001	29	Reset Module without SBIT	Recommended
	0101010	2A	Module IBIT	Recommended
	0101011-0101111	2B-2F	Reserved	Reserved
Module I/O Control and Test (MICT)	0110000	30	Disable Module I/O	Recommended
	0110001	31	Enable Module I/O	Recommended
	0110010	32	Force Module Outputs	Recommended
	0110011	33	Sample Module-No Change	Recommended
	0110100	34	Sample Module-Don't Care	Recommended
	0110101	35	Sample Module with Force	Recommended
	0110110	36	Release Module I/O	Recommended
	0110111-1001111	37-4F	Reserved	Reserved
HiRelPCI Extensions	1010000	50	Disconnect module from HiRelPCI Bus	Required
	1010001	51	Connect Module to HiRelPCI Bus	Required
	1010010	52	Disable main power converters	Required
	1010011	53	Enable main power converters	Required
	1010100	54	Read Serial Number, NodeId	Required

Table 6—Maintenance Bus Commands

Command Class	Command Code (Binary)	Command Code (HEX)	Command	Status
	1010101	55	Failure Insertion Control (simulation)	Required
	1010110	56	TBD	
	1010111	57	Read Power Status Block	Required
	1011000	58	Set Poke Address and mode (64 bits)	Required
	1011001	59	Read Poke Data (64 Bit mode)	Required
	1011010	5A	Write Poke Data (64 bit mode)	Required
	1011011	5B	TBD	
	1011100	5C	Read 1149.1 JTAG data	Required
	1011101	5D	Write 1149.1 JTAG Data/Program Data	Required
	1011110	5E	Read Message (Header + Data + CRC)	Required
	1011111	5F	Write Message (Header + Data + CRC)	Required
User-Defined	1100000-1111110	60-6E	User-Defined Commands	Reserved

for HiRelPCI are added as commands 50 to 5F. The Maintenance Bus (MB and MTM are used in this document) is attached to all elements in a common chassis. This extends to all boards, power supplies and fans that support a physical backplane which may contain up to 2 segments. There are two candidates for the Maintenance Bus functions, they are:

0.8 Supporting structures

0.8.1 Serial Interconnect

In addition to the primary bus, there are additional communication systems on the backplane. These include a 10 Megabit Ethernet (10Base2), and lines reserved for IEEE 1394-1995 (Firewire) and the Maintenance Bus.

Ethernet provides communications between the boards in the system and through a hub located on the Central Service Module (CSM) to the outside world for a low cost connection between bus systems.

Firewire (IEEE 1394-1995) can provide read/write capability to the boards in the system when a redundant path is needed with a single main bus. Boards that use this system of redundancy would all need to support the 1394 interface. Firewire is a multimaster bus and can be used when more than one processor is available.

IEEE P1394.2 is added to the system through a bridge in one or more of the bus slots. As P1394.2 devices become available, the bridge may be added to the CSM function.

0.8.2 Support Signals

Support signals on the backplane include:

CCLK10M - 10.0000 MHz Constant Clock line (accuracy to be determined)
INTA# - An Interrupt Request line. May not be supported by most processors.
REQP0# - REQP3# - Bus Request Priority Request Pins.

CCLK10M, Constant clock line, has a frequency of 10.00 MHz and is used as a reference frequency. This frequency may also be used as the clock for the IEEE Std 1149.5 MTM maintenance bus. The bus clock in this system has a frequency range for 0 to 66.66Mhz and may use the 0 Hz for debugging, and power conservation functions, and can not be counted on as present for board level functions.

A legacy INTA# line is retained. This is only one line and its use is discouraged.

0.9 Electrical Specifications

Several different specification are used within this standard: 1) the LVTTL 3.3V signaling levels of the main PCI style parallel structure; 2) GTL signaling for the TDM bus; 3) Ethernet ECL signal levels for the ethernet and 4) Firewire signal levels for the IEEE 1394-1995 bus.

0.9.1 Connector Pin Assignments

The first pinout shown in Table 7 is for the normal bus module that connects to any position on the

Table 7—Non-CSM Position Connector Pin Assignments

	a	b	c	d
1	P48VA	FGND	P48VA	P48VA
2	P48VA	FGND	N48VA	N48VA
3	N48VA	P48VAPRE	N48VA	POWERONA
4	P48VB	N48VAPRE	P48VB	POWERONB
5	P48VB	P48VBPRE	P48VB	N48VB
6	N48VB	N48VBPRE	N48VB	N48VB
7	Resv’d	GND	1394CLK	1394DATA
8	AD32	GND	AD33	SAD15
9	AD34	GND	AD35	AD36
10	AD37	GND	AD38	AD39
11	AD40	GND	AD41	SAD14
12	AD42	GND	AD43	AD44
13	AD45	GND	AD46	AD47
14	AD48	GND	AD49	SAD13
15	AD50	GND	AD51	AD52
16	AD53	GND	AD54	AD55
17	AD56	GND	AD57	SAD12
18	AD58	GND	AD59	AD60
19	AD61	GND	AD62	AD63
20	PAR64	GND	C/BE4#	SAD11
21	C/BE5#	GND	C/BE6#	C/BE7#
22	ACK64#	GND	REQ64#	CCLK10M
23	AD00	GND	AD01	SAD10
24	AD02	GND	AD03	AD04
25	AD05	GND	AD06	AD07
26	C/BE0#	GND	M66EN	SAD09
27	AD08	GND	AD09	AD10
28	AD11	GND	AD12	AD13

Table 7—Non-CSM Position Connector Pin Assignments

	a	b	c	d
29	AD14	GND	AD15	SAD08
30	C/BE1#	GND	PAR	SERR#
31	SBO#	GND	SDONE	PERR#
32	LOCK#	GND	STOP#	SAD07
33	IRDY#	GND	TRDY#	DEVSEL#
34	FRAME#	GND	C/BE2#	AD16
35	AD17	GND	AD18	SAD06
36	AD19	GND	AD20	AD21
37	AD22	GND	AD23	IDSEL
38	C/BE3#	GND	AD24	SAD05
39	AD25	GND	AD26	AD27
40	AD28	GND	AD29	AD30
41	REQ#	GND	AD31	SAD04
42	SAD03	GND	Resv'd	INTA#
43	GNT#	GND	ENET	Resv'd
44	SAD01	GND	MCLK	SAD02
45	CLK	GND	REQP0#	SAD00
46	REQP1#	GND	REQP2#	RST#
47	MMD	GND	MSD	REQP3#
48	MPR	GND	MCTL	Spare5#
49	user defined	user defined	user defined	user defined
50	user defined	user defined	user defined	user defined
51	user defined	user defined	user defined	user defined
52	user defined	user defined	user defined	user defined
53	user defined	user defined	user defined	user defined
54	user defined	user defined	user defined	user defined

bus other than for the CSM module position, the use of rows 49 to 54 are define by the board and connect through on the backplane to provide user I/O with a flexible connection

Central Service modules require the additional pins to provide the clocks and arbitration for the bus segment

Table 8—CSM POSITION CONNECTOR Additions

	a	b	c	d
48				BPSN#
49	CLKS0	CLKS6	REQ0#	GNT0#
50	CLKS1	GNT6#	REQ1#	GNT1#
51	CLKS2	REQ6#	REQ2#	GNT2#
52	CLKS3	GND	REQ3#	GNT3#
53	CLKS4	PUPOWER	REQ4#	GNT4#
54	CLKS5	PUPOWER	REQ5#	GNT5#

of up to 8 slots. The above chart shows the changed definitions for a 7 slot backplane entity.

On 12su boards an additional set of 72 pins are located in the center of the board and are defined for the TDM bus and the service modules clocks for the TDM bus and the redundant TDM structure. The pinouts for this connector are:below. The second set is for the normal board case of not being in the CSM position.

Table 9—CSM Connector

	a	b	c	d
7	ATCLK0	GND	ATCLK6	BTCLK3
8	ATCLK1	GND	ATCLK7	BTCLK4
9	ATCLK2	GND	BTCLK0	BTCLK5
10	ATCLK3	GND	BTCLK1	BTCKK6
11	ATCLK4	GND	BTCLK2	BTCLK7
12	ATCLK5	GND	1.5VPU	1.5VPU

	a	b	c	d
1	ATDM0	GND	ATDM1	ATDM2
2	ATDM3	GND	ATDM4	ATDM5
3	ATDM6	GND	ATDM7	BTDM0
4	BTDM1	GND	BTDM2	BTDM3
5	BTDM4	GND	BTDM5	BTDM6
6	ATDMCLK	GND	AFRAME	BTDM7
7	User Defined	User Defined	User Defined	User Defined
8	User Defined	User Defined	User Defined	User Defined
9	User Defined	User Defined	User Defined	User Defined
10	User Defined	User Defined	User Defined	User Defined
11	User Defined	User Defined	User Defined	User Defined
12	User Defined	User Defined	User Defined	User Defined
13	CTDM0	GND	CTDM1	CTDM2
14	CTDM3	GND	CTDM4	CTDM5
15	CTDM6	GND	CTDM7	DTDM0
16	DTDM1	GND	DTDM2	DTDM3
17	DTDM4	GND	DTDM5	DTDM6
18	CTDMCLK	GND	CFRAME	DTDM7

Additional configuration options are under consideration that will allow for more rear I/O from the board. Within the 24pin blocks additional configurations are available the include single RF or Fiber I/O and up to 6 RF/Fiber connectors per block using smaller diameter coax/fiber. These configurations include:

1. 6su board with only 32 bits of address and data (opens up about 36 I/O lines)
2. 12su board with out redundant bus or TDM (frees middle connectors and lower connectors.
3. 6su and 12su boards with mechanical keying to support the use of Fiber and RF connectors.
4. 18su and 24su boards with additional sets of connectors.

Part of the effort here is to prevent these boards from plugging into destructive conditions. For this purpose the board that have RF or Optical connectors in place of the normal pin I/O shall have connectors keyed to prevent the insertion of the normal pin I/O into the backplane positions with the RF/OPTICAL connectors

0.9.2 Power Distribution

The power paradigm for this system is the distribution of redundant wide tolerance main voltage with local voltage regulation as needed. The distribution power rails are DC isolated from the incoming power supply to meet isolation requirements of 3750V with required creepage and clearances distances. It is also expected that the onboard regulators will also be DC isolated from the power rails with the only common element from node to node being signal ground.

This power is distributed through dual power rails, each rail can deliver up to 4 Amps of power at a nominal voltage of 48V to each board slot. This nominal 48V supply has a range of 36V to 58V. This stays within the definitions of “Safety Extra Low Voltage” that will comply with IEC 950 and EN 60 950 for European requirements and UL1450 for US requirements. This voltage provides sufficient power while reducing the current density in the connector pins. In telecommunication system the voltage would be a nominal 52.8V to 55V with normal batteries under charging conditions.

Additional precharge lines are located on longer pins to bring the input circuits up to voltage before the main power pins connect. The precharge pins are current limited to 100 mA for safety on the long pins. The last pins to make contact on each set of power rails is the power-on pins to start the onboard power converters.

Power rail A contain 11 pin:

Table 10—A Power Rails

Positive Rail	Negative Rail	Voltage Difference	Maximum Current	Number of pins
P48VA	N48VA	36VDC to 58VDC	4 Amperes	4 pins per Rail
P48VAPRE	N48VAPRE	36VDC to 58VDC	0.1 Ampere	1 pin per Rail
POWERONA	N48VA	0 to 15VDC	20 mA	1 pin

Power rail B contain 11 pin:

Table 11—B Power Rails

Positive Rail	Negative Rail	Voltage Difference	Maximum Current	Number of Pins
P48VB	N48VB	36VDC to 58VDC	4 Amperes	4 pins per Rail
P48VBPRE	N48VBPRE	36VDC to 58VDC	0.1 Ampere	1 pin per Rail
POWERONB	N48VB	0 to 15VDC	20 mA	1 pin

The remaining two pins in the first block of 24 pins are FGND = Frame Ground. This ground is used on a strip around the board and contacts the grounding clips on the card guides. Frame Ground is isolated from common signal ground. Overall the power block of 24 pins looks like this:

Table 12—Power Pin Locations on connectors

Row\Column	a	b	c	d
1	P48VA	FGND	P48VA	P48VA
2	P48VA	FGND	N48VA	N48VA
3	N48VA	P48VAPRE	N48VA	POWERONA
4	P48VB	N48VAPRE	P48VB	POWERONB
5	P48VB	P48VBPRE	P48VB	N48VB
6	N48VB	N48VBPRE	N48VB	N48VB
Length	**6.5 mm**	**8 mm**	**6.5 mm**	**5.75 mm**

0.10 Mechanical Specifications

0.10.1 Mechanical Sizes

This standard uses the Hard Metric mechanical system with the following features:

IEC 917-2-2/IEEE Std 1301-1992 standard dimensions
Board top surface offset 10 mm from left reference on module (from the front panel)
Board position allows front and back component placement (7.23mm back, 19mm front)
30 mm front panel allows 1 inch disk drives on boards

0.10.1.1 HiRelPCI Connectors

2mm Connectors - FutureBus style - Metral style
- Bellcore, UL, CSA approved
- IEC 1076-4-OX (48B) compliant
- EIA SP3179 compliant
- Stackable connectors for I/O
- 8x24 short pin = Berg Part Number 70235-977 or equivalent
- 1x24 short pin = Berg Part Number 70232-977 or equivalent
- 1x24 Long pin for rear plug = Berg Part Number 70232-987 or equivalent
- Standard RF and Optical I/O available for I/O connector positions
- Keying available to prevent damage when mixing RF and pin I/O

Staggered Pin Height to support Live Insertion
- A Row = 6.5mm
- B Row = 8.0mm
- C Row = 6.5mm
- D Row = 5.75mm

Signal return path for every 2 signals.

6su boards contain
- 216 pins - 4 column of 54 pins including 24 user defined I/O pins

12su boards contain
- 504 pins - 4 columns of 126 pins including 72 user defined I/O pins and TDM blocks

0.10.1.2 HiRelPCI board formats

6su HiRelPCI
- 6su = 115mm (4.53") x 213mm depth (8.39")

12su HiRelPCI
- 12su = 265mm (10.43") x 288mm depth (11.34")

0.10.1.3 HiRelPCI board size comparison to VME style boards

6su HiRelPCI ~ 3u VME style
- Board Size -115mm x 213mm vs. 100mm x 160mm
- Board Area - 245 sq. cm vs. 160 sq. cm raw size
- Usable Area - 430 sq. cm vs. 140 sq. cm component area

12su HiRelPCI ~ 6u VME style
- Board Size - 265mm x 288mm vs. 233.35mm x 160mm
- Board Area - 763 sq. cm vs. 374 sq. cm raw size
- Usable Area - 1416 sq. cm vs. 336 sq. cm component area

0.10.2 Environmental

P1996 is intended to operate in the following environmental conditions:
- Temperature -40C to +85C
- Humidity 0 to 100%
- Altitude -100m to +15000m

Cooling
- Convection cooling for transportation and other severe environmental applications.
- Forced air cooling may be used in telecom and other less demanding environmental applications.