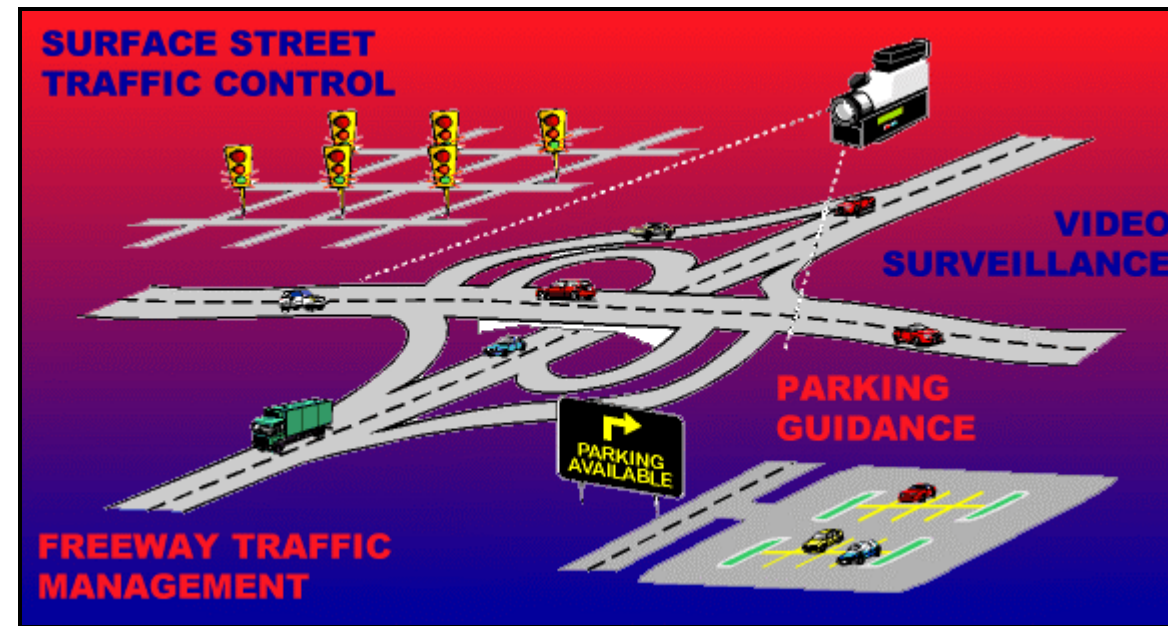




Hi-Rel PCI Market Watch

High Reliability and Extensibility with PCI and SCI
Will it be the Next Wave in Industrial-Computer Buses?



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Market Segment Manager*



HiRelPCI

IEEE P1996 Standard for an Extensible High Reliability Enhanced PCI Bus

Introduction

High Reliability PCI, or HiRelPCI bus as it is called, was developed from a basic need to provide a highly reliable, highly available industrial-type computer system for transportation controls and telecommunications systems. Transportation and traffic control systems demand very low system failure rates, despite their severe environments. Traffic controls must operate faultlessly 24 hours a day, seven days a week on street corners from northern Alaska to the deserts of Arizona despite harsh and often hostile conditions. Although telecommunications systems are not exposed to environments quite as severe, they are alike in the need for Reliability, Availability and Maintainability (RAM). Additionally, there is a need in telecommunications for time-division multiplexing (TDM) in the computer bus for telecom circuit switching of data, per the international Synchronous Digital Hierarchy (SDH), at rates defined in ANSI T1.105. Both applications require redundant capabilities to allow continuous operation with a single fault. Other applications that may be attracted to this type of redundant bus could include business critical applications such as financial, medical, or industrial embedded-computer systems.

All of these applications require a method to extend beyond the local bus to other similar type buses in a uniform redundant manner. The solution for this redundant requirement was to include a provision in the bus to handle the message packets of the IEEE Standard 1394 called Fire Wire, and the IEEE Standard 1596 called SCI. This provision allows uniform 64-bit address packets to be sent to addressable 64K nodes. For more demanding multi-processor systems, the cache coherency properties of SCI could be employed as needed.

HiRelPCI bus was specifically designed to satisfy the following requirements:

1. **Reliability** - through passive backplanes, redundant busses, and redundant power.
2. **Availability** - through design for no single point of failure.
3. **Maintainability** - through an **MTM** (maintenance) bus, hot-swap, standby modules.
4. Scalability - through a **Packet Bus** to 1394 and SCI, circuit-switch I/O to STS-12.
5. Performance - Packet Bus performance to 533 Mbytes/s with up to 95% efficiency.
6. Redundancy - no single point of failure on a normally configured system.
7. Industrial/Automotive temperature range operation - 40° C to + 85° C.
8. +48 nominal power distribution for efficiency.
9. Configuration management - through CSR Architecture, FireWire and MTM bus.
10. Redundant connectivity - through backplane FireWire and 10Base2 Ethernet.

How Does it Work?

The HiRelPCI bus standard is a combination of properties taken from other standards and modified to provide the structure to meet the needs described above. The elements that make up this highly reliable, highly available bus include:

1. A Parallel system-bus using PCI-style signaling for normal bus access.
2. A Packet Bus added on top of the parallel bus for packet switched connections.
3. A Time-Domain Multiplexed bus for circuit switched connections.
4. A Maintenance bus for control of system resources for hot swap operations.
5. An addressing structure that uses 64-bit address blocks.
6. Several supporting interconnection systems.
7. A set of electrical specifications for low voltage signaling, GTL + signaling and power.
8. A set of mechanical specifications to provide a well defined enclosure system.

The Combination of Properties Builds a System that Provides...

- Extensibility to 64,000 nodes of 256 terabytes each.
- IEEE 1212 CSR architecture for easy expansion via SCI, FireWire, and 1394.2, etc.
- Redundant functions to provide no single point of failure for continuous operation.
- Hot Plugging of any board to replace faulty modules or to upgrade features.
- Circuit Switched base for audio, telephony, video, ATM.
- Packet Switched connection model for shared memory operations via SCI/CSR.

What is FireWire?

FireWire is a high-speed serial bus designed for low-cost, multi-host operation. Work started on what was then called "SeialBus" in 1986, when Apple engineers defined a serial bus to handle most of the Macintosh peripherals. Further work was done on the bus by a number of companies, including IBM. The resulting bus has become the IEEE Standard 1394-1995. When IBM's interest deteriorated, the slack in FireWire was taken up by the 1394 Trade Association. The Trade Association's goal was for FireWire to become the serial bus for consumer electronics, as well as the high-speed serial link for computers, and eventually provide the mechanism to link products from these two markets together. The increasing digitization of consumer electronics opened the door for FireWire. For instance, FireWire could link a camcorder to a VCR, the VCR to the TV, and the VCR to a stereo or a set-top box, as well. It could also connect these units to a PC to integrate computing with home entertainment.. Intel has commented that it expects to incorporate FireWire into the Intel chipsets and motherboards sometime in 1999.

Bus Signal Definitions

Normal bus signaling on the P1996 (HiRelPCI) bus is based on the PCI Local Bus Specification 2.1 using 3.3V signals. This provides leverage on all the silicon built to support the PCI market — the same strategy used by CompactPCI bus. P1996 protocol is flexible and provides smooth performance from 0 to 533 Mbytes/s throughput for read and write burst transactions.

The PCI bus was also extended to include a packet mode, called Packet Bus, to support the packets sent over the SCI and Serial Express busses that extend communications to other elements in a redundant system. Packet operations are transparent to the normal

PCI transactions compliant to Rev 2.1. HiRelPCI can operate in Packet Bus mode, normal PCI mode, or a mix of both modes.

Each component in the system is attached to the Maintenance Bus which is a bus defined by IEEE Standard 1149.5-1995.

CSM Function

Centralized resources needed for bus operations are supplied by the Central Services Module (CSM). There is one CSM for each bus segment.

The Central Services Module provides the following services for the bus:

- Clock Drivers for each slot on the bus segment.
- Bus Arbitration for each slot on the bus segment
- Repeater Hub for the Ethernet signals
- Repeater Hub for the 1394-1995 FireWire serial bus
- Possible Bridge to IEEE P1394.2 Serial Express bus
- PCI to PCI Bridge if needed
- Possible Time-Domain Multiplexer interface between outside world and backplane bus
- TDM to TDM Bridge and framing store if needed
- Clocks for the TDM slots when used
- System Monitor Functions
- Maintenance Bus Master

What is Serial Express?

Serial Express is best described as an extension to the processor/memory bus, extending outside the motherboard chassis. Although Serial Express uses point-to-point duplex cabling, between nodes, the protocol uses a backplane heritage. Many of the Serial Express protocols were leveraged from other cable-friendly IEEE bus standards such as IEEE 1596 (SCI), and IEEE Standard 1394 (Fire Wire). Some properties were derived from Fire Wire, such as unaligned larger byte-aligned transfers, Isochronous, fixed-rate time-latency data transfers, and multi-speeds for different links. Other properties were derived from SCI, like scalability, concurrent data transfers, smaller 64-byte packets, fast arbitration, ringlets around each packet, and isochronous multicast distribution to multiple nodes. Serial Express uses read/write transactions to transfer data between nodes. Bridges can extend read/write transactions allowing them to be forwardable. Each Serial Express cable has a flipped pair of input and output signals communicating concurrently (full duplex). For example, A (Tx) to B (Rx) and B (Tx) to A (Rx). For short distances, signals are transmitted over a 150 ohm twisted pair copper cable. Data is processed when passing through each attached node, removing signal noise and clock jitter. Signal processing circuits detect unconnected or redundant cable ports, and electronically bypass these unused ports. Specific node identifiers are also assigned to each node during a bus reset, so there is no need for the user to set DIP switches. The resulting bus has become the IEEE Standard 1394-2.

Packet Bus Operation

Packet Bus operations are added to the basic parallel bus structure to improve the performance of the system with a split mode of operation. This mode is also known as “write only mode” bus operation in that each request and response is a write transaction. The basic function is to free the bus resources during the time needed to fetch or process the data at the target end of the transaction. Packet mode operation does not impose any additional requirements on the participants as buffers handle the packets to and from the bus.

Packet Bus operation is optional for the HiRelPCI bus. This mode can be used to produce the highest bandwidth operations on the bus with a greater than 4 gigabit throughput a reality.

Time-Division Multiplexing (TDM) Bus Operation

Dual TDM busses are included as an option for telecommunications usage. The TDM bus follows the structure of ANSI T1.105-1991 using the blocking factors used in the international standard. The standard provides a reference for multiple embedded carriers and provides an internationally accepted framework for circuit presentation and ATM integration if needed. Basic timing is provided by the CSM board position and consists of clocks with less than 1ns of skew and a framing pulse to define the local chassis time slot count. Simulations indicate possible clock speeds to 77.76 MHz using GTL logic to provide an upper limit of STS-12 on each of the sets of data lines.

12su systems would have dual TDM blocks for reliable redundant operation. Each of these busses has 2-byte wide paths that may be used as input streams and are each readable and writeable on each time period. Each time cycle has a 12.86ns duration which requires a terminated GTL+ bus to reduce reflections and lower the propagation delay to incident wave travel.

What is SCI?

Scalable Coherent Interface (SCI) is effectively a combination computer backplane bus, processor memory bus, I/O bus, high-performance switch, packet switch, ring, mesh, local area network, optical network, parallel bus, serial bus, information sharing, information communication system that provides distributed directory-based cache coherency for a global shared memory model. It uses electrical or fiber optic point-to-point duplex cables. SCI began in 1988 during the IEEE P896 Futurebus project when some individuals realized that not even the best bus design would be able to support the needs of multi microprocessors a few years down the road. In order to scale the performance up to far higher levels, SCI abandoned the bus-specific parts of the Futurebus protocol that could not be scaled, but kept the general Futurebus architecture so as to easily interface with Futurebus subsystems. Features were added to make it easier to interface to other common busses like VMEbus and the PCI bus, and to I/O connections such as ATM and Fibre Channel. Typical performance is currently in the range of 200 to 1000 Mbytes/s over distances of tens of meters with electrical cables and kilometers with fiber optic cables. SCI was completed in 1991, and became IEEE Standard 1596.9.

Maintenance Bus Operation

The maintenance Bus Master issues sets of commands that are described in the IEEE Standard 1149.5-1995. The Maintenance Bus (MTM) is attached to all elements in a common chassis. This applies to all boards, power supplies and fans that support a physical backplane which may contain up to 2 segments. The are two candidates for the Maintenance Bus functions, they are:

The IEEE Standard 1149.5 MTM Bus defined for use in avionics and other similar systems by the same standards group that provided the IEEE 1149.1 JTAG testing functions.

The second candidate is an undefined 2 wire differential serial bus that uses an HDLC protocol bus with message layer.

The Maintenance Bus controls the following functions:

- Reads board-unique identifiers
- Reads board configuration ROM
- Reads board slot identifiers
- Connects and disconnects board from bus
- Controls board power
- Performs built-in self test (BIST) functions
- Performs the JTAG testing of the boards
- Reads/writes IEEE 1212-1991 Address spaces
- Controls diagnostic systems testing such as induced failures
- Controls any other functions requested by board designs

Node Addressing

Extension beyond a single PCI Bus is required for applications that need a few more, or vastly more processors, memory, and I/O boards. Connectivity beyond a single system is greatly enhanced by addressing a card slot on a bus segment as a node. Each slot has a node address consisting of 16 bits, split into 3 bits of slot ID and 13 bits of address assigned by a switch on the backplane or by a bridge to the SCI and Serial Express node address. While this does allow for 8192 bus segments of 8 slots each, the use of all slots on a backplane will limit 16 slots per chassis and therefore limit the number of chassis to 4096.

Supporting Structures

Serial Interconnect

In addition to the primary bus, there are additional communication systems on the backplane. These include a 10MB Ethernet (10Base2), and lines reserved for IEEE 1394-1995 (Firewire) and the Maintenance Bus (MTM, or the undefined 2-wire). The Maintenance Bus also provides a very low speed interconnect between the boards and the support equipment for the purpose of maintaining and testing the bus.

10Base2 Ethernet provides communication between the boards in the system and through a hub located on the Central Services Module (CSM) to the outside world for a low cost connection between bus systems.

Firewire (IEEE1394-1995) can provide read/write capability to the boards in the system when a redundant path is needed with a single main bus. Boards that use this system of redundancy would need to support the 1394 interface. Firewire is a multimaster bus and can be used when more than one processor is available.

Serial Express (IEEE1394.2) is added to the system through a bridge in one or more of the bus slots. As P1394.2 devices become available, the bridge may be added to the CSM function.

Electrical Specifications

Several different specifications are used within the HiRelPCI Standard.

- LVTTTL 3.3V level for the main PCI parallel bus
- GTL signaling for the TDM bus
- Ethernet ECL signal levels for the Ethernet
- Firewire signal levels for the IEEE 1394-1995 bus.

Power Distribution

The power paradigm for this system is a distribution of redundant wide-tolerance main voltage with a local voltage regulation as needed. The distribution power rails are DC isolated from the incoming power supply to meet isolation requirements of 3750V with required creepage and clearance distances. The onboard regulators will also be DC isolated from the power rails with the only common element from node to node being signal ground.

This power is distributed through dual power rails. Each rail can deliver a +48V nominal power supply at up to 4 amps to each board slot. The nominal voltage supply has a range of +36V to +58V. This remains within the definitions of "Safety Extra Low Voltage" complying with IEC 950 and EN 60 950 for European requirements, and UL 1450 for US requirements. The nominal +48V voltage provides sufficient power while reducing the current density in the connector pins. For telecommunications systems the voltage would be a nominal +52.8V to +55V, with backup batteries under charge conditions.

Mechanical Specifications

Mechanical Sizes

The standard uses the "Hard Metric" (HM) mechanical system with the following features:

- IEC 917-2-2 / IEEE Standard 1301-1992 standard dimensions
- Board top surface is offset 10 mm from left reference on module (from front panel)
- Board position allows front and back component placement (7.23 mm back, 19 mm front)
- 30 mm front panel allows for 1 in. disk drives on boards

HiRelPCI Connectors

2mm HM Metral™ (Futurebus) pin and socket type

Bellcore, UL, CSA approved

IEC 1076-4-OX (48B) compliant

EIA SP3179 compliant

Stackable connectors for I/O

8 x 24 short pin [BERG p/n 70235-977, or equivalent]

1 x 24 short pin [BERG p/n 70232-977, or equivalent]

1 x 24 long pin for rear plug [BERG p/n 70232-987, or equivalent]

Standard R/F and optical I/O available in I/O connector positions

Keying available to prevent damage when mixing R/F and pin I/O

Staggered Pin Height to support Live Insertion

Row A = 6.5 mm

Row B = 8.0 mm

Row C = 6.5 mm

Row D = 5.75 mm

Signal Return Path for every 2 signals

6su boards provide:

216 pins (4 columns of 54 pins including 24 user defined I/O pins)

12su boards provide:

504 pins (4 columns of 126 pins including 72 user defined I/O pins and TDM blocks)

HiRelPCI Board Formats

6su HiRelPCI Boards:

115 mm [4.53 in.] x 213 mm [8.39 in.] in depth

12su HiRelPCI Boards:

265 mm [10.43 in.] x 288 mm [11.34 in.] in depth

HiRelPCI Board Sizes Compared to VME Boards

6su HiRelPCI ~ 3u VME

[115 mm x 213 mm] versus [100 mm x 160 mm] with VME

12su HiRelPCI ~ 6u VME

[265 mm x 288 mm] versus [233.35 mm x 160 mm] with VME

Environmental Specifications

Operating Temperature Range

- 40° C to + 85° C

Humidity

0 to 100% RH

Altitude

- 100 m to +15000 m

Cooling

Convection cooling for transportation and other severe environmental applications.

Forced air cooling for telecom and other less demanding environmental applications.

System Configurations

Small System - 2 to 8 Nodes, with 1 Level Interconnect

- Serial Express Interconnect
- PacketBus Interconnect
- SCI Interconnect

Medium System - 4 to 8 Nodes, with 2 Level Interconnect

- Serial Express Interconnect 3 to 4 Busses
- PacketBus / Serial Express Interconnect
- Serial Express / PacketBus / SCI Interconnect

Medium System - 4 to 8 Nodes, with Redundant Links

- Serial Express Interconnect 3 to 8 Busses
- PacketBus / Serial Express Interconnect
- Serial Express / PacketBus / SCI Interconnect
- Multiple Servers - Multiple Disk Arrays

Large System - 20 to 4096 Chassis, 20 to 64K Nodes, Multiple Redundant Links

- Serial Express Interconnect 3 - 100+ Busses
- PacketBus / Serial Express Interconnects
- Serial Express / PacketBus / SCI Interconnect
- 2 to 4 Links / PacketBus
- Different types of Links



Corporate Sponsorship

Intersection Development Corporation

Corporate sponsorship for HiRelPCI began with Intersection Development Corporation, of Downey California. When IDC came on the scene, they saw a long-standing industry that was literally at a crossroad. There were many small specialized suppliers of traffic and transportation control products, but there was virtually no focus on integrated systems. The ability of small companies to support major projects was often questioned. IDC's fundamental concept was to create a vehicle to unify an industry force. A year after IDC was formed, they embarked on an ambitious acquisition program, aimed at combining small suppliers into a bigger, stronger organization. In parallel with work on products that adhered to traditional National Electrical Manufacturers Association (NEMA) and 170 specifications, IDC's development group also led the NEMA effort to create a National Standard Transportation Protocol. IDC is currently chairing the NEMA technical committee to develop the *National Transportation Communication for ITS Protocol* (NTCIP). This protocol will be designed into future transportation equipment, and is the key communication protocol of the FHWA's Intelligent Transportation System (ITS) projects. IDC maintains a separate engineering center that strictly focuses on new product development that stays at the leading edge of traffic control.

Summit Computer Systems, Inc.

When IDC recently abandoned sponsorship for HiRelPCI due to economic difficulties, the slack was quickly picked up by Summit Computer Systems, Inc. of Los Gatos, California. Summit realized the significance of HiRelPCI as a bus standard for High Reliability, Non-Stop industrial computer systems. In alliance with telecommunication giants Tandem Computers Incorporated, and Centigram Communications Corporation, Summit has established itself as the primary market driver and corporate spearhead to take the HiRelPCI standard to ballot. This effort is led by Summit executives Bob and Patrick Davis.

Berg Electronics and ViaSystems have joined Summit in their sponsorship for HiRelPCI as a viable solution for a High Reliability Non-stop computer bus.

For technical information and standards updates on HiRelPCI contact:

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Markets

What is the Market for HiRelPCI?

Many will ask - *Who are the customers for HiRelPCI?* The answer is simple... there are none... yet. And, *What about all the hoopla for CompactPCI as the "hot" new industrial computer bus?*

It's true that CompactPCI also does what HiRelPCI does - leverage the low-cost silicon from the desktop computer world. However, keep in mind that CompactPCI was brought to market primarily with this objective - cost, cost, cost. CompactPCI offers high-horsepower, low-cost, multi-processor computing, along with high availability and reliability through its hot swap capability. And true, CompactPCI is more robust than desktop PCI when used in harsh industrial environments. For these reasons, CompactPCI was quickly adopted by the telecommunications and embedded computer industries. What CompactPCI does not do, is offer a 99.99% non-stop system. For example, a bullet fired through a CompactPCI processor board or backplane will most likely take down the system.

HiRelPCI on the other hand, is directed at a similar, but yet very different market. HiRelPCI does what CompactPCI can do, and more. It is being brought to market with a different feature in mind - reliability, reliability, reliability.

Traffic Control Systems

For instance, in the case of Emergency Vehicles, the payoff is in saved lives and property, in fewer traffic accidents involving emergency vehicles. In fact, avoiding the legal settlement from a single accident can more than pay for an entire emergency traffic preemption system for some cities. In the case of transit vehicles, the payoff is in increased safety, reduced travel time, better adherence to schedules, and ultimately in increased ridership.

A Word about Traffic Preemption Systems

Earlier types of traffic preemption systems like strobe-based, radio-based, sound-based, and transponder-based systems each had their own advantages and disadvantages. With strobe-based systems, light sources other than strobes can cause false preemption. Routine maintenance is required to keep the optical surfaces clean, replace lamps and keep the optical path clear. With radio-based systems all intersections within radio range receive the same preempt direction, sometime with cataclysmic results. Sound-based systems have a relatively short range, and performance is affected by the sound level of the sirens, ambient noise, surrounding structures and the weather. Transponder-based systems provide the accuracy required for transit vehicles, but are not responsive to vehicle speed. Their main drawback is that a very expensive infrastructure of powered, active transponders is required wherever vehicles are to be detected. Also, once in place, this infrastructure is quite inflexible.

Leading edge technology systems use GPS satellite and two-way radio to provide green traffic signals to emergency vehicles and transit vehicles such as busses and light rail. It is an all-weather, non-stop system that uses advanced technology to handle the most complex approaches and routes, including curves and sharp corners. It provides error-free preemption timing based on estimated time of arrival.

License plate matching has long been used by transportation engineers and planners as a source for data for origin-destination (O-D), travel time and other studies. These studies typically require large numbers of staff, high associated costs, and would take several months to collect, analyze and document the results. Manual operations often produce unacceptably high error rates in data collection and processing; especially when large amounts of data needed to be collected and analyzed in a short period of time. Many of the shortcomings associated with manual collection and processing of data from vehicle license plates can be overcome through the use of high-end video camcorders and machine vision license plate readers. A camcorder can be placed over the roadway looking across three to four lanes of traffic. These systems are called Traffic Analysis Systems (TAS). TAS provides lane-by-lane data on the number, class, speed, and density of the traffic flow and roadway occupancy. In addition, automatic license plate readers can be installed in roadside cabinets near the cameras, typically using one license plate reader per camera. Using this set-up, the video images of license plates are captured, compressed, automatically read, and stored as bitmap and ASCII files for later use. Typically, these output files are transmitted to a remote location for review and further handling. TAS generates data files that include the time, license plate, location, lane number, vehicle occupancy, distinction between commercial and private vehicle, and direction of traffic flow. Movement patterns of five-axle tractor-trailer trucks, and USDOT and ICC number information can also be collected off the sides of the tractor cab doors of interstate haulers by the use of high-speed video technology. This information is used by the DOT for documentation and marketing purposes.

The result of the automatic analysis is a very thorough, fast and data-rich traffic survey. This approach often yields match-rates ten to twenty times higher than traditional license plate O-D and travel time methods. Video derived traffic data is statistically robust and can provide improvements in traffic flow by means of comparing the travel time measurements of traffic during peak versus non-peak hours, or general purpose lanes versus adjacent HOV (express) lanes. As congestion on major urban interstate and arterial roadways continues to grow, the need to monitor the travel time along routes normally taken by commuters, and their alternative route choices, is becoming increasingly apparent.

Many video-based survey applications can be designed around the automatic collection and processing of vehicle license plates at parking facilities or for special events such as major league sports, shopping malls, airport passenger drop-offs and pick-ups, intersections, grade crossings, traffic queues, bridge crossings, and many others.

Intersection monitoring and turning movement studies are frequently needed as a tool to more effectively and efficiently control the movement of vehicles through an interchange.

Telecommunications

Computing systems that support the telecommunications industry, on both the network and the business management sides, must be reliable and scalable to deal with the explosion of services. They must also provide the bandwidth and performance needed to handle the Internet and other media-rich applications. HiRelPCI's open architectural approach and fundamental availability and scalability make it the clear choice for the more demanding applications in the telecommunications industry.

The merging of telephone network and internet technology will enable a broad range of integrated services across multiple disciplines and platforms. Intelligent Network (IN) technology will be the driving force behind the revolution in network-based services, providing the infrastructure on which future telecommunications services will be based.

Airtime fraud can be a costly problem for wireless providers. In the past, operators could only detect fraudulent access, and the process involved labor-intensive post-call analysis. By implementing a computer-based Authentication Center (AC), providers can effectively detect and prevent fraud before it happens - and without affecting their legitimate subscribers. Home Location Registers (HLR) are high-performance off-switch databases that let subscribers roam without service interruption and enables them to use intelligent network service features previously available only in their local calling area.

Enterprise-Class Clustering

Massively parallel NonStop Himalaya Servers (Tandem Computers) have been performing as cost-effective, highly fault-tolerant, highly scalable cluster computers for decades. These systems are built from loosely coupled, shared-nothing processors - each with its own memory and copy of the operating system - the same architecture type embraced by part of the Microsoft Cluster Server (MSCS) phase II multinode clustering initiative. Cluster computing has recently been extended to incorporate the benefits of *Windows NT Server* open standards with the existing Unix-based systems and *Non-stop Software* (a proven suite of cross-platform clustering middleware for business-critical applications). Using this open application development environment, software developers can create powerful applications for Himalaya servers from desktop computers using familiar development tools.

Himalaya Intelligent Network Servers provide enhanced service for telecommunications, wireline, and wireless providers that require high-volume, fault-tolerant intelligent network database servers and call processors.

Messaging and Communications Solutions

Two principal business sectors are targets for HiRelPCI in the voice processing market.

The Customer Premise Equipment (CPE) business sector includes corporations, government agencies, universities and other large organizations.

The Service Provider (SP) business sector includes Wireline (PTT, RBOC, independent telcos, and cable telephony companies), and Wireless Service Providers (cellular, PCS, GSM, CDMA and paging companies).

Messaging and Communication integration enables users to access and interact with a broad range of information in a variety of formats - including voice, text, data, and fax - all from a touch tone telephone, personal computer or wireless device. VoiceMemo® is a feature-rich voice messaging product that provides call processing, telephone answering, paging and audiotext services for thousands of users. VoiceMemo also includes, as an option, an automated attendant that answers, screens and forwards calls 24 hours a day. It also allows callers to select from a menu of call-routing options, and provides direct extension dialing. VoiceMomo systems can be integrated with nearly all major PBX and central office systems in nearly all languages.

FaxMemo™ is a fax messaging product that integrates with VoiceMemo to provide users with fax store-and-forwarding capabilities from their VoiceMemo mailboxes. CallAttendant® combines powerful call processing and flexible automated attendant capabilities to meet the specific call processing needs of any company, department or individual user. Fully integrated with VoiceMemo, CallAgent® answers calls, plays

messages and routes callers without human intervention. OneView™ is a multi-media desktop product that allows users to create, play, answer and forward voice, fax and compound voice and fax messages from their PCs, extending the benefits of voice messaging from telephone to the desktop. OneView operates under Microsoft Windows to give users point-and-click access to multimedia messages by listing them in a single "inbox". OneView Remote™ is a product that allows subscribers to access their messages from their PC using a telephone line and modem, extending the benefits of OneView to the laptop computer for mobile users.

Potential Customers for HiRelPCI

Who Would Use HiRelPCI?

As discussed earlier, HiRelPCI will not share the same markets as CompactPCI, nor will CompactPCI share the same markets with VME. HiRelPCI will appeal only to high-end customers requiring extremely powerful, highly fault-tolerant and super-scalable systems with no single point of failure. These applications could include critical business systems for financial institutions including banks and the stock market; critical medical systems for life support and patient monitoring; High Reliability, Non-Stop industrial and embedded computer systems, such as for Terminal Doppler Weather Radar (TDWR); air traffic control (ATC), aircraft Instrument Landing Systems (ILS); and other critical applications such as Enterprise data servers for Data Centers and mass storage systems.

HiRelPCI was first developed for use in the traffic control system environment. Below are the top 10 traffic control system manufacturers involved in Intelligent Traffic Systems (ITS) technology:

- Eagle Traffic Control Systems (Business Unit of Siemens) - Austin, TX
- Econolite Control Products, Inc. - Anaheim, CA
- Emergency Preemption Systems, Inc. (EPS) - Scottsdale, AZ
- Microcom, Pty. Ltd. - Fremantle, Australia
- Midwest Traffic Products, Inc. - Romeoville, IL
- Peek Traffic Systems, Inc - Sarasota, FL
- The Revenue Markets, Inc. (TRMI) - Accord, NY
- RTC Manufacturing, Inc. - Dallas/Ft. Worth, TX
- Transformation Systems, Inc - Houston, TX
- Science Applications International Corporation (SAIC) - San Diego, CA

Telecommunications companies showing interest in HiRelPCI because of its packet addressing capability include Tandem Computers Incorporated and Centigram Communications Corporation. Other companies expressing interest in HiRelPCI, but have not yet committed to supporting the bus include: IBM, Pro-Log, Sun Microsystems, and Dialogic Corporation.

Conclusion

P1996 HiRelPCI is a practical bus solution for Highly Reliable, Highly Scalable Systems. There are few, if any HiRelPCI systems in place at this time, as a result of low visibility in the marketplace and few corporate sponsors. The standard has been at a virtual standstill for the preceding 6 to 8 months. Conversely, CompactPCI's success story was the result of its high visibility and corporate sponsorship from companies like Intel, Microsoft, Motorola, Pro-Log, Force Computers, and its designer, Ziatech.

CompactPCI revenues are forecasted to climb rapidly in 1998 through 2000 to over \$1 Billion by the year 2001, say industry observers. As a result of the earlier bus wars, it has been determined that CompactPCI Bus will not actually compete with, but rather will compliment VME Bus. CompactPCI is targeted at the commercial telecommunications, and embedded computer market segment because of its features such as processor independence, leverage on low-cost silicon technology from the desktop PCI world, availability of a myriad of commercially available I/O boards, hot swap capabilities, and more. VME on the other hand, will continue to dominate proprietary, high-end systems for the military, and high-end commercial systems requiring true multi-processor power and real-time operating system capability. VME's projected market revenues are said to top \$2 Billion by year 2001.

HiRelPCI Revenues

The target revenues for HiRelPCI systems, based on the market segments identified and discussed in this report are calculated at approximately 5 to 10% of the CompactPCI market revenue, or about \$50 to 100 Million - of which the connector content could reach between \$1 and 2 Million. The projected selling price of HiRelPCI is approximately that of CompactPCI + 20%.

Our Role at Berg

We would certainly be wise to develop a market for HiRelPCI. Why? — because Berg has a “drop-in” product – the Metral™ four-row, pin-and-socket connector. Aside from supplying samples and technical support there is no significant investment on our part; however there is a great deal to gain. Additionally, the HiRelPCI initiative provides opportunities for other Berg products and for our sister divisions, as well. We have a sister division ViaSystems that sells backplanes. ViaSystems has joined us in supporting HiRelPCI in partnership with Summit Computer Systems, and has agreed to build a working backplane to present to customers like IBM, Lucent, NCR, or anyone looking for a High Reliability industrial bus backplane. ViaSystems has a front end opportunity to sell the finished backplanes pre-loaded with Berg Metral connectors.

With allied interest and support for the P1996 standard from Berg, Summit, and ViaSystems, along with Tandem's interest in its packet capabilities, and Centigram's interest in its super-scalability, the standard could be ready for feasibility testing as early as June 1998.